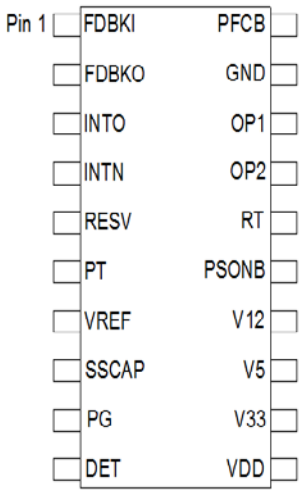
Description

The EST9001A is designed with a LLC control circuit and a complete power supervisor using at the switched mode power supply.
It contains various supervisor functions, like under voltage protection, over voltage protection, power good output and power supply ON/OFF control.
UVP and OVP function is for +3.3V, +5V, +12V outputs and PG is a power good signal to inform external device. PSONB controls the SMPS ON/OFF.
The LLC function controls the frequency of main power by the different load consumption.

PIN CONFIGURATION (Top View)



DIP-20/SOP-20

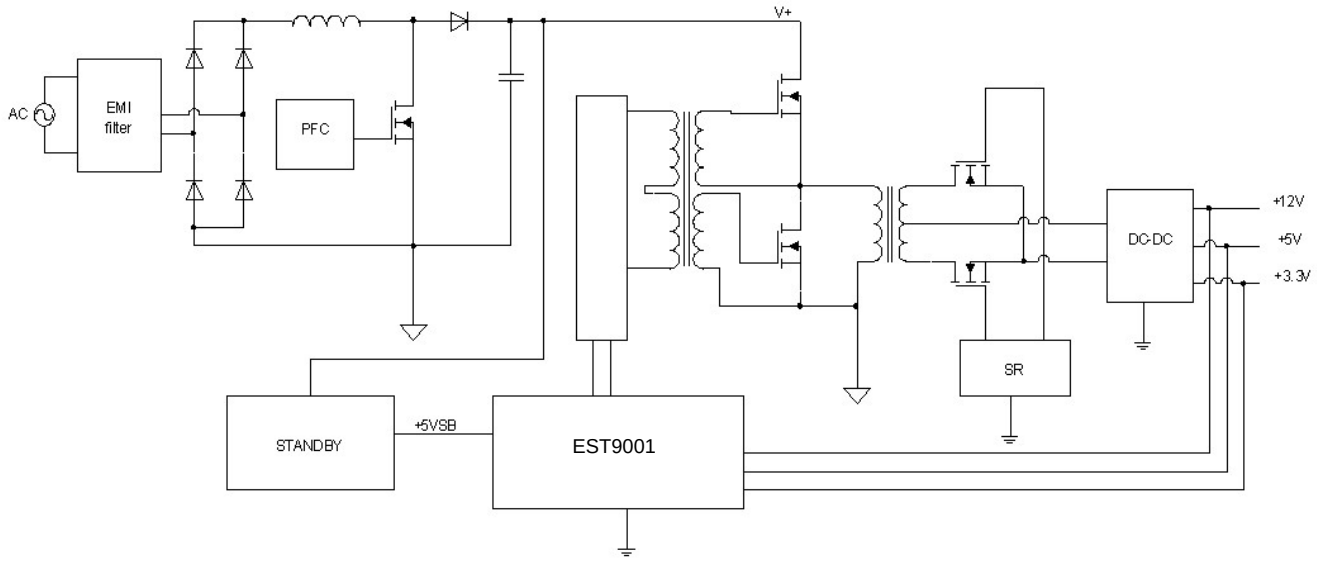
FEATURE

- 3-channel under voltage protection (UVP)
- 3-channel over voltage protection (OVP)
- 1-channel extra protection (PT)
- 1-channel sense input to control the PG (DET)
- SMPS on/off control function (PSONB)
- Dual output for Driver operation (OP1/OP2)
- Enable/Disable PFC function operation (PFCB)
- VDD under voltage lockout
- 20-Pin package
- Pb-free Package are available

ORDERING INFORMATION

ORDER NUMBER	Package	Shipping	Top Marking
EST9001AAD	DIP-20(Pb-free)	Tape	EST9001AAD
EST9001AAS	SOP-20(Pb-free)	Tape & Reel	EST9001AAS

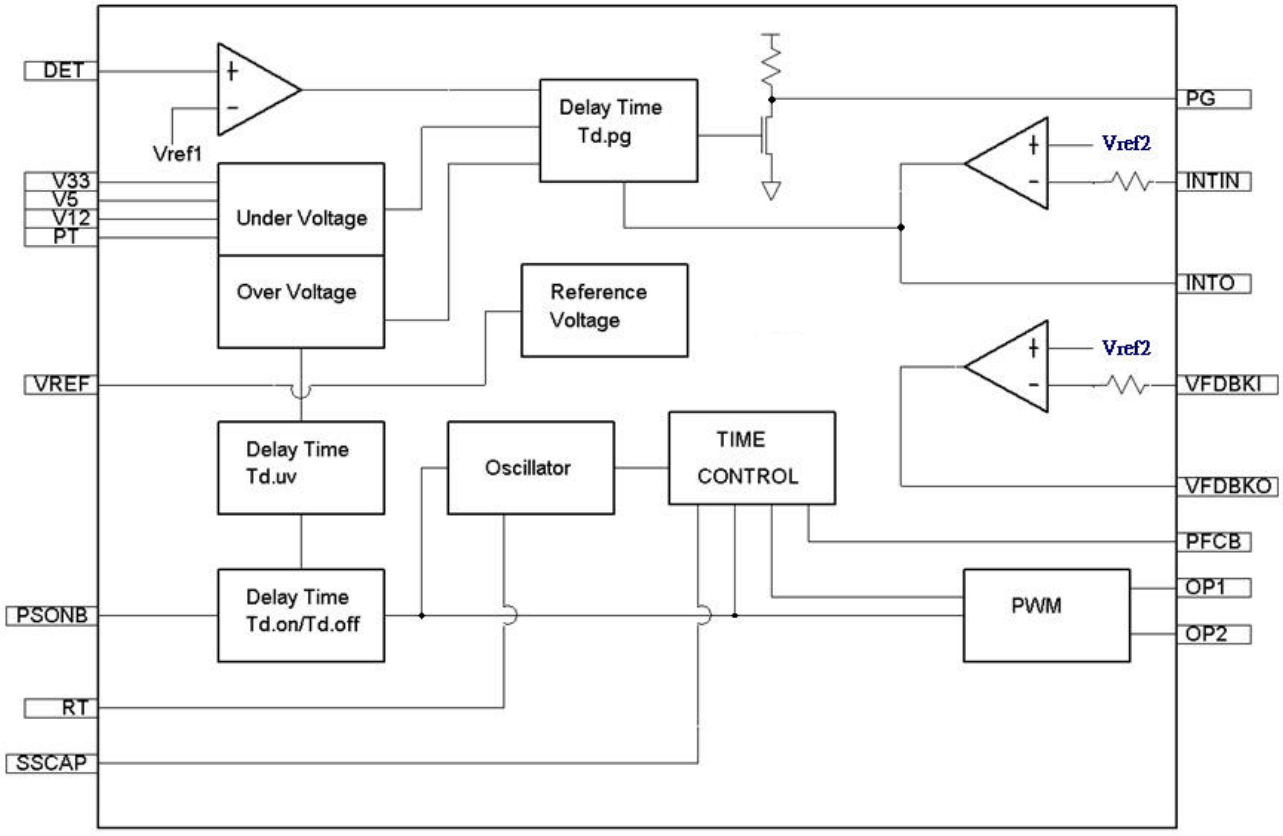
REFERENCE APPLICATION CIRCUIT



PIN DESCRIPTION

Pin	Symbol	Type	Function
1	FDBKI	I	Amplifier FDBK input
2	FDBKO	O	Amplifier FDBK output
3	INTO	O	Amplifier INT output
4	INTN	I	Amplifier INT input
5	RESV	-	Reserve
6	PT	I	Protection signal input
7	VREF	-	Reserve
8	SSCAP	O	Set by an external capacitor connected to GND
9	PG	O	Power good signal
10	DET	I	Sense signal input
11	VDD	-	Supply voltage
12	V33	I	OVP, UVP for +3.3V
13	V5	I	OVP, UVP for +5V
14	V12	I	OVP, UVP for +12V
15	PSONB	I	Remote ON/OFF control
16	RT	O	Frequency set by an external resistor connected to GND
17	OP2	O	Primary side Driver2 output
18	OP1	O	Primary side Driver1 output
19	GND	-	Ground
20	PFCB	O	Active low signal to Enable/Disable PFC function operation, the delay time from PSONB to PFCB is set by SSCAP

FUNCTION BLOCK DIAGRAM



*Note-1: In some application circuits, adding a resistor in series with the PSONB pin could reduce the noise spike and avoid the pin from damage

*Note-2: EST reserves the right to make changes without notice to improve the function specification

ABSOLUTE MAXIMUN RATINGS

PARAMETER		MIN	MAX	UNITS
Supply Voltage	VDD	-0.3	7	V
Input Voltage	V33,V5,V12,PT,FDBKI,INTI,PSONB,DET	-0.3	7	V
Output Voltage	RT,OP1,OP2,FDBKO,INTO,PSONB,SSCAP,PG, PFCB	-0.3	7	V
Operating Temperature Range	T_O	-20	+85	^oC
Storage Temperature Range	T_S	-65	150	^oC

ELECTRICAL CHARACTERISTICS (For VDD=5V and Tj=25 ^oC)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage Protection (OVP- V33,V5,V12)						
Over voltage threshold	OV33		3.8	4.1	4.4	V
	OV5		5.8	6.2	6.6	V
	OV12		4.4	4.6	4.9	V
Noise debounce time	Tg.ov			510		us
Under Voltage Protection (UVP- V33,V5,V12)						
Under voltage threshold	UV33		1.7	1.9	2.2	V
	UV5		2.7	3.0	3.3	V
	UV12		2.1	2.4	2.7	V
Noise debounce time	Tg.uv			110		us
SSCAP						
Source current	Isscap			50		uA
VDD Under Voltage Lockout (UVLO)						
Start-up voltage				4		V
PSONB *Note						
High level input voltage	V_{IH}		1.8			V
Low level input voltage	V_{IL}				0.7	V
PSONB input delay time	Td.on/off			40		ms
PSONB						
Delay time	Tpsonb.on/off			35		ms
PG, DET, PT, PFCB						
PG delay time from PSON	Td.pg		180	280	380	ms
PG internal pull high resistor	Rpull.up		3.76	4.7	5.64	KΩ
Sink current PG	Ipg.sink	VPG=0.7V		20		mA
Sink current PFCB	Ipfcb.sink	VPFCB=0.7V		22		mA
DET over voltage threshold	Vdet.ov		2.75	3.0	3.25	V
PT under voltage threshold	Vpt.uv		2.75	3.0	3.25	V
RT						
Source current	IRT	RT=100 KΩ		12		uA
OP1, OP2						
Push Pull output	Fosc	RT=100 KΩ		40		KHz
INTN, INTO						
INTP Internal voltage	Vintp			2.50		V
INTN input voltage	Vintn		0		5	V
INTN input series resistance	Rintn			370		Ω
FDBKI, FDBKO						
FDBKP Internal voltage	Vfdbkp			2.50		V
FDBKI input voltage	Vfdbki		0		5	V
FDBKI input series	Rfdbki			370		Ω

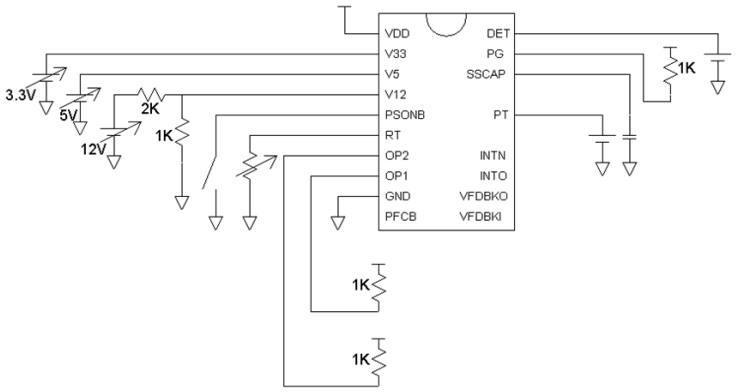
resistance						
VREF						
Reference output voltage	VREF			3.00		V
Total Device						
Supply current	I_{CC}	PSONB= 5V		4		mA

TIMING DIAGRAM

REMOTE ON/OFF & PG

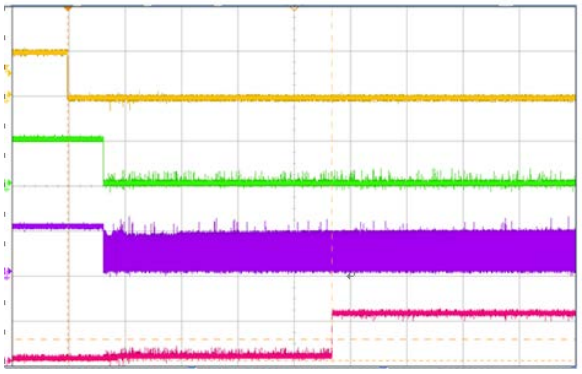
When the PSON active, the output signals from OP1 & OP2 drive the coil and the V33, V5, V12 raise the voltage. If all of the V33, V5, V12 raise to the correct voltage level within the limited time, the PG will raise from low to high voltage level. This PG will inform the device, like PC motherboard, to initiate the system. If one of the voltage does not raise to the correct voltage level within the limited time, the PG will be at low voltage level.

If the PSON active the power supply and initiate the system successfully, the EST9001A supervises all the output voltage continually. When the PSON disable the EST9001A at the high voltage level, the PG will be low level and the OP1 and OP2 raise to an always high level.



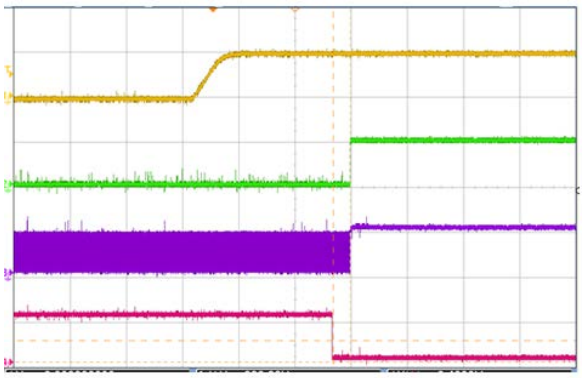
CH1(Y-PSON);CH2(G-PFCB);CH3(P-OP1);CH4(R-PG)

*@ REMOTE ON



CH1(Y-PSON);CH2(G-PFCB);CH3(P-OP1);CH4(R-PG)

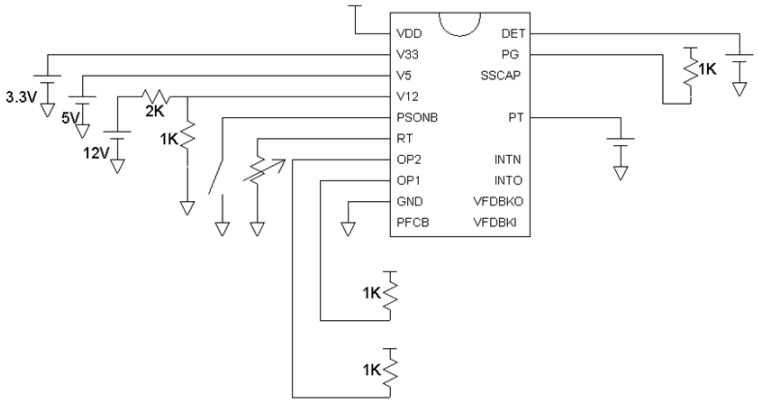
*@ REMOTE OFF



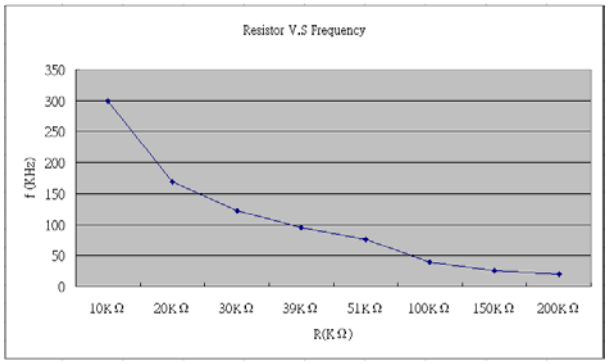
Oscillator

The OP1 and OP2 frequency is set by the external resistor connected from the PIN-6(RT) to GND. When the external resistor is 100KΩ, the output frequency at each of the OP1 and OP2 is about 40KHz.

Change the resistor value of the VR connected at the RT, the different frequency can be got from the OP1 and OP2.



R	I(μA)	f(KHz)
10KΩ	127	300
20KΩ	60	169
30KΩ	42	122
39KΩ	32	95
51KΩ	25	75.8
100KΩ	113	39.5
150KΩ	8.4	26.3
200KΩ	6.5	20.3

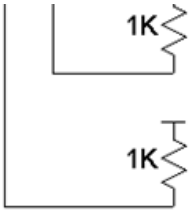


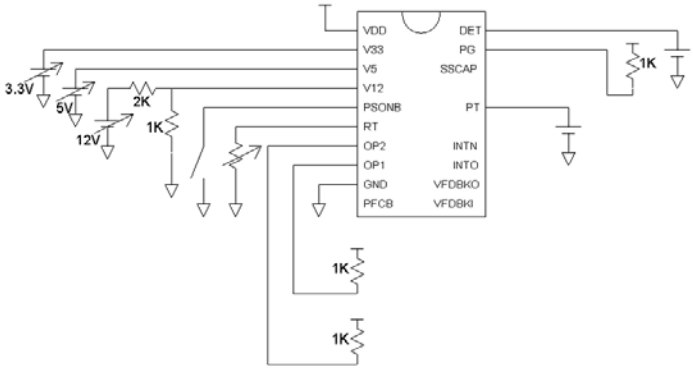
In general, the LLC frequency is changed by the load, the frequency range is about in the range of 20KHz to 250KHz.

For reference example, the frequency range is about from 22KHz to 245KHz. The frequency is 52.4KHz at 550W of the full load and 91.7KHz at 10W of the light load.

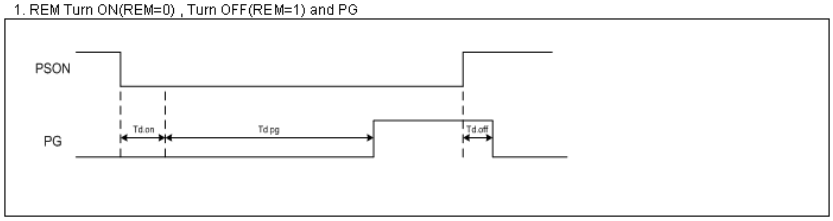
The frequency at different loads are listed as below for reference,

	(10W)	20%(110W)	50%(275W)	70%(385W)	100%(550W)
PWM 頻率 (KHz)	91.7	66.2	59.5	56.2	52.4

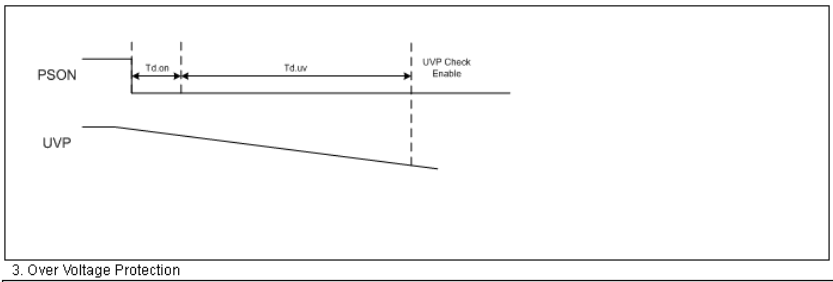




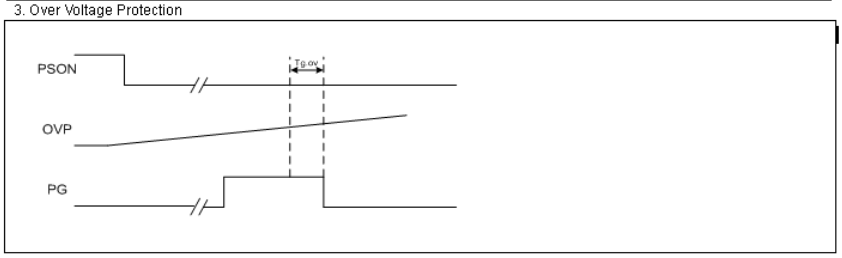
1. REM Turn ON(REM=0) , Turn OFF(REM=1) and PG



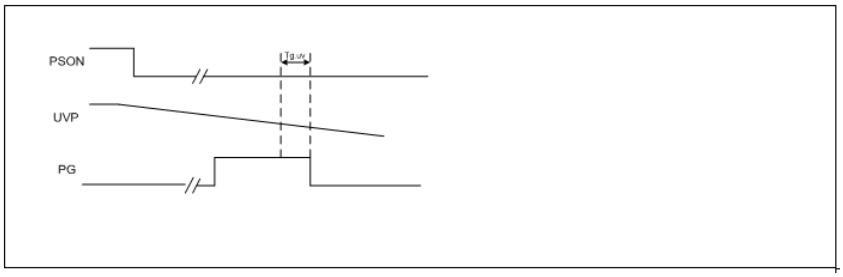
2. REM vs. Under Voltage Protection Delay time



3. Over Voltage Protection



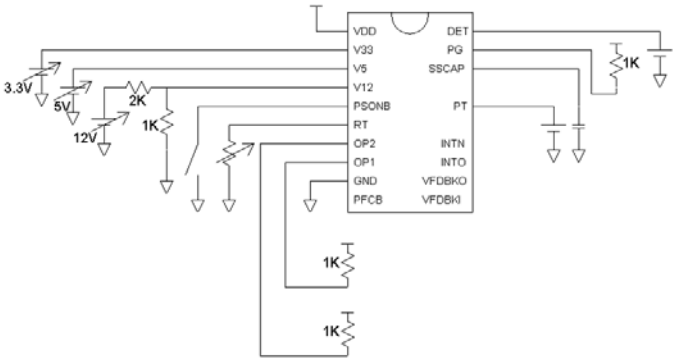
4. Under Voltage Protection



PFCB

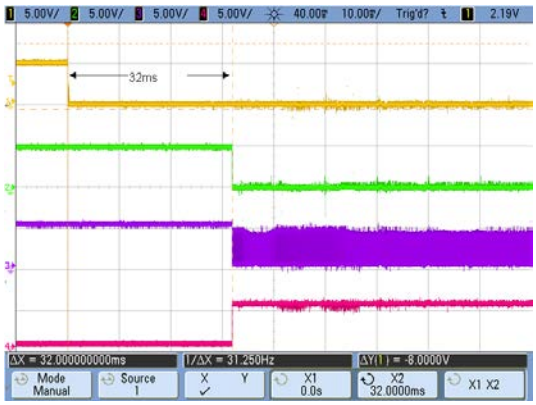
The PFCB can be used to inform the PFC circuit to work. The delay time between PSONB and the PFCB is determined by the external capacitor that connected from SSCAP to GND. The source current of the SSCAP is 50uA. When the SSCAP capacitor value is 0.1uF, the reference waveform and delay time is as below,

$$T = \frac{C*V}{I} = \frac{10^{-7}*5}{50^{-6}} = 10ms$$

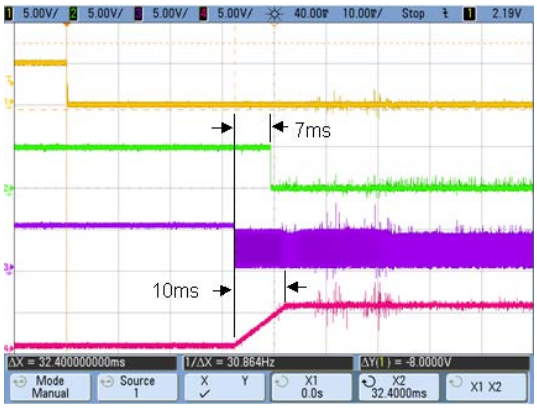


CH1(Y-PSON);CH2(G-PFCB);CH3(P-OP1);CH4(R-SSCAP)

*SSCAP=None



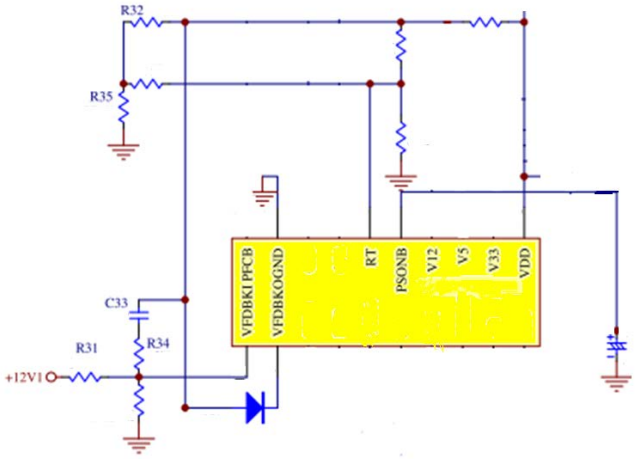
*SSCAP=0.1uF



OP amplifier feedback function

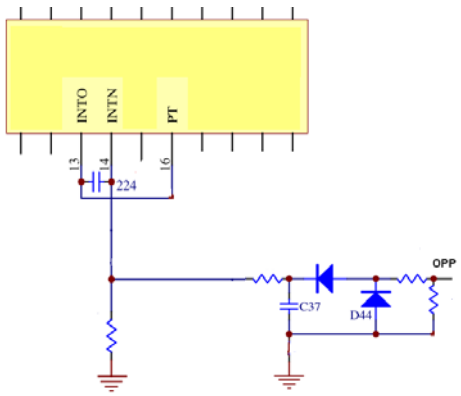
EST9001A build in the OP amplifiers for the power control functions. For example, the OP amplifier can be used as the output voltage feedback loop control to keep all the output voltage in stable voltage range at different load. Through the feedback control, the feedback voltage can be used to vary the OP1 and OP2 frequency by the change of load.

The feedback circuits can be done through the divided 12V voltage connected to the VFDBKI and the RT resistors circuit connected to the feedback loop.



OP amplifier OPP function

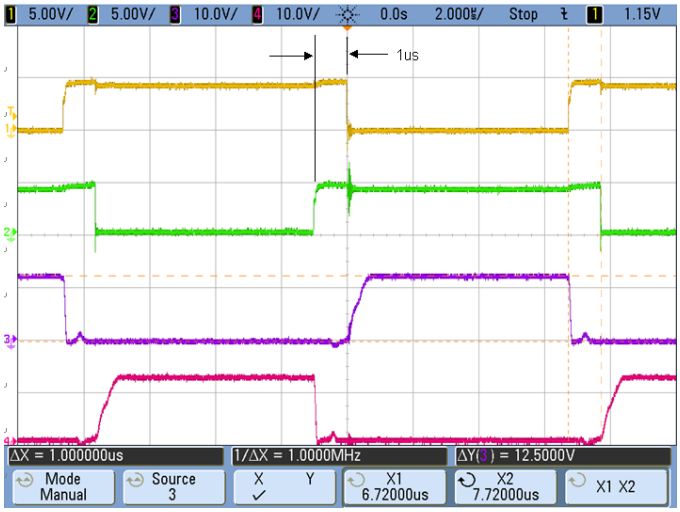
The suggestive OPP circuit can be implemented as the circuit below. Connected a capacitor between the INTI and INTO can reduce the noise interference and PT will detect OPP signal from the induction coil.



PFM and SR function in the power supply

Reference to the real power supply circuit that use EST9001A as the controller, the dead time between the OP1, OP2 and the SR is about 1us. The dead-time at the real power circuit should be designed carefully for the different load.

*CH1/CH2:OP1/OP2 signal, CH3/CH4: SR control signal



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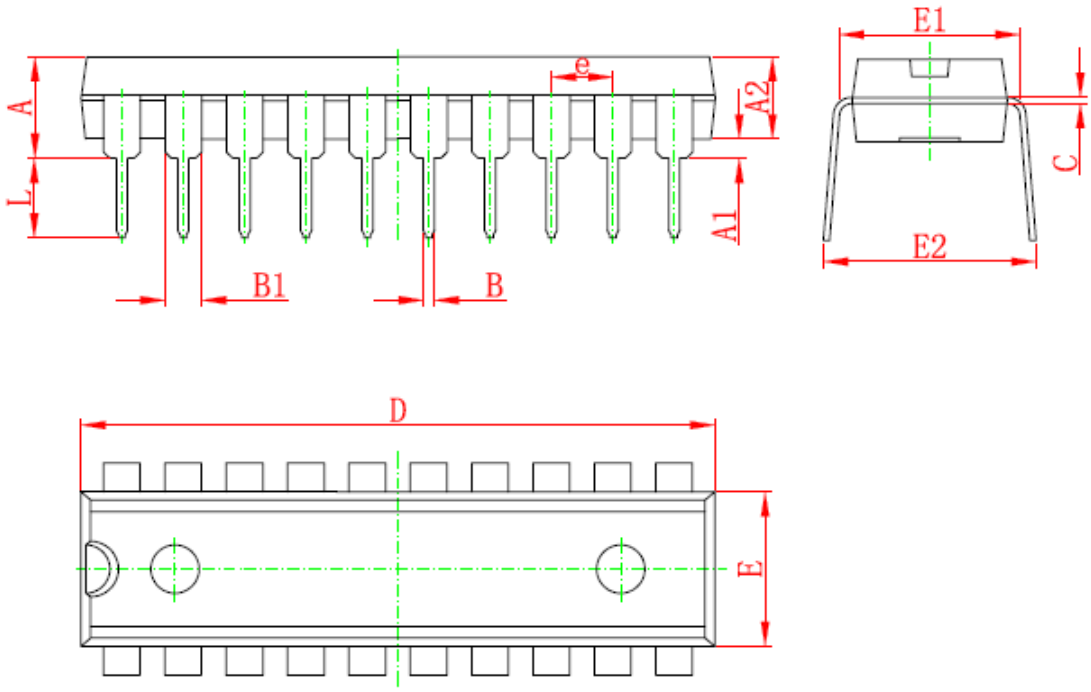

inch / mm

Symbols	Dimensions In inches		Dimensions In millimeters	
	Min.	Max.	Min.	Max.
A	------	0.184	------	4.674
A1	0.014	------	0.356	------
A2	0.119	0.150	3.023	3.810
B	0.013	0.023	0.330	0.584
B1	0.060 (TYP)		1.524 (TYP)	
c	0.008	0.015	0.203	0.381
D	0.961	1.097	24.409	27.864
E	0.232	0.273	5.893	6.934
E1	0.300 (TYP)		7.620 (TYP)	
e	0.100 (TYP)		2.540 (TYP)	
L	0.112	0.149	2.845	3.785
E2	0.307	0.393	7.798	9.982