

Description

EST7630F is higher integrated circuit incorporates all advanced sensing function to protect from over and under voltage a four-channels protection supervisor (3.3V/5V/ and double12V).

The function of Over Current Protection (OCP) monitors output currents through sense resistor by using smart comparator circuit is more exact and easy.

EST7630F provide the fault protection latch (FPOB), a power good output (PGO), the PSONB control and the power good input control (PGI).

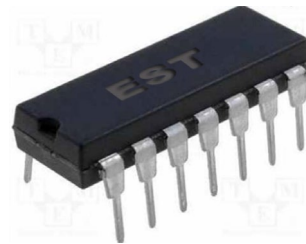
Features

- The Over/Under Voltage Protection for 3.3V/5V and double 12V
- The Over Current Protection monitors 3.3V/5V and double 12V output currents and related lockout
- Both of fault protection output and power good output are open drain output stage
- 75ms delay for SPS short circuit protect
- 2ms PSONB input signal de-bounce
- 73us for OVP noise immunity de-bounce.
- 150us for internal noise immunity de-bounce
- 125ms power good delay time for PGO
- 4ms time delay between PGO and FPOB when PSONB turn off

Application

- PC SPS line housekeeping IC (3.3V, 5V, and 12V)
- Industry Computer
- Mining Pool Power

Pin Assignments



DIP-14L

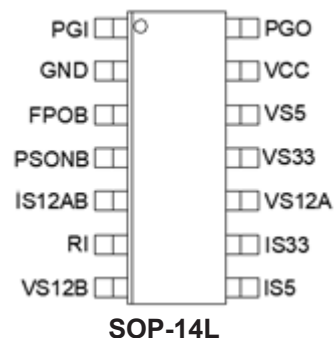
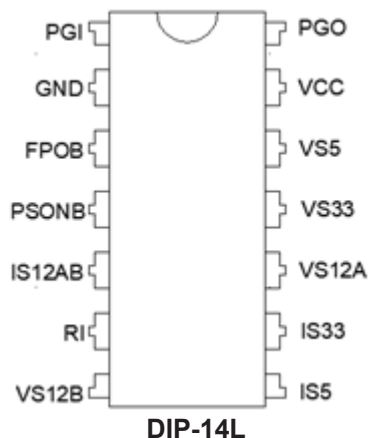


SOP-14L

Ordering Information

Order Number	Package Type	Packing	Top Marking
EST7630F	DIP-14 (RoHS)	Tube	EST.7630F
EST7630FS	SOP-14 (RoHS)	Tube	EST.7630FS
EST7630FSR	SOP-14 (RoHS)	Tape & Reel	EST.7630FS

Pin connection (Top View)

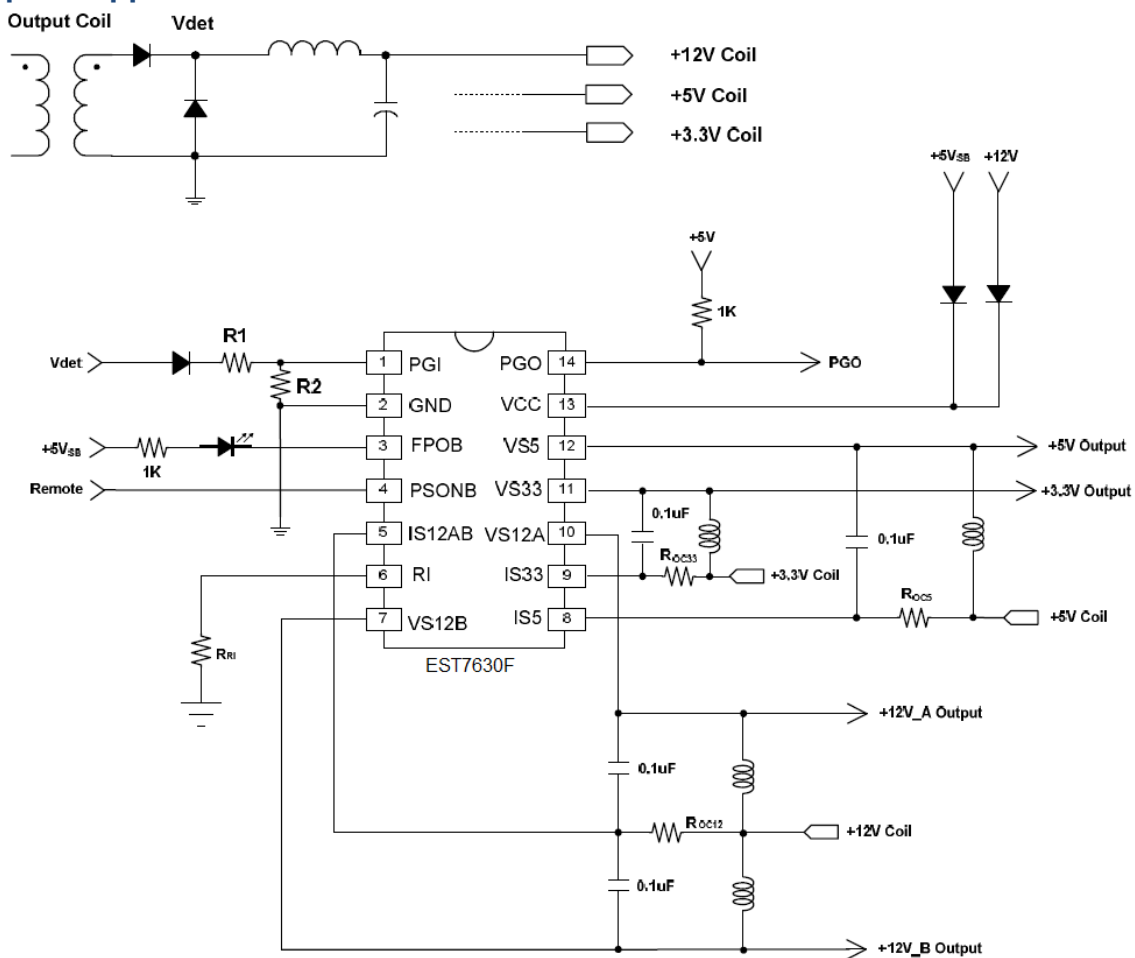


SPS Secondary Supervisor IC

Pin Description

No.	I/O	Designation	Description
1	I	PGI	Power good input signal pin
2	I	VSS	Ground
3	O	FPOB	Inverted fault protection output ,open drain output stage
4	I	PSONB	Remote ON/OFF switch input pin
5	I	IS12AB	12V over current protection sense input pin(A/B)
6	O	RI	OCP reference current setting pin
7	I	VS12B	12V over/under voltage protection input pin(B)
8	I	IS5	5.0V over current protection sense input pin
9	I	IS33	3.3V over current protection sense input pin
10	I	VS12A	12V over/under voltage protection input pin(A)
11	I	VS33	3.3V over current protection sense input pin
12	I	VS5	5.0V over/under voltage protection input pin
13	I	VCC	Power supply
14	O	PGO	Power good output stage

Typical Application Circuit



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Remark
Storage Temperature (Tstg)	---	-40 to 140	°C	
Operating Temperature (Topr)	---	-25 to 85	°C	
Junction Temperature (Tj)	---	150	°C	
Supply Voltage (VCC)	VCC	-0.5 to 18		
Output Voltage Range (VO)	VS12A, VS12B, IS12AB	-0.5 to 16	V	
	VS5, IS5, VS33, IS33	-0.5 to 8		
	PGI	-0.5 to 8		
	PSONB,	-0.5 to 8		
Output Voltage Range (VO)	FPOB	-0.5 to 16	V	
	PGO	-0.5 to 8		
	RI	-0.5 to 8		
Junction-to-Ambient Thermal Resistance*	θ_{JA}	95	°C/W	DIP-14
Junction-to-Case Thermal Resistance**	θ_{JC}	25	°C/W	
Junction-to-Ambient Thermal Resistance*	θ_{JA}	125	°C/W	SOP-14
Junction-to-Case Thermal Resistance**	θ_{JC}	37	°C/W	
Power Dissipation (@TA<50°C)	PD	800	mW	DIP-14
		600	mW	SOP-14

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Free standing with no heatsink; without copper clad. (Measurement condition – just before junction temperature Tj enters into OTP)

**Measure on the PKG top surface

DC Electrical Characteristics (VCC =12V, Ta=25)

Input Power Supply:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	4.3	12	16	V	
Supply Current	Icc		1.0	2.0	mA	VPSON = 0V
Reset Threshold Voltage	VIH	2.9	3.2	3.5	V	HIGH→LOW

Over-Voltage function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Over-Voltage Threshold	OVT _{VS33}	3.70	3.90	4.10	V	
	OVT _{VS5}	5.70	6.10	6.50	V	
	OVT _{VS12}	13.10	13.80	14.50	V	For VS12A and VS12B

Under-Voltage function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Under-Voltage Threshold	UVT _{VS33}	2.00	2.20	2.40	V	
	UVT _{VS5}	3.30	3.50	3.70	V	
	UVT _{VS12}	8.50	9.00	9.50	V	For VS12A and VS12B

Over-Current function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Offset voltage	V _{OS33}	-4	0	2	mV	Offset voltage between IS and VS
	V _{OS33}	-4	0	2	mV	
	V _{OS33}	-4	0	2	mV	
IS pin sink current	I _{leak}	155	160	165	uA	RI Resistance=62.5KΩ

PSONB, Analog Input function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Threshold Voltage		1.60			V	LOW→HIGH
				1.0	V	HIGH→LOW
OP hysteresis voltage	VHV1	0		50	mV	

PGI, Analog Input:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Threshold Voltage of PGI		0.60	0.65	0.70	V	Enable UVP
		1.16	1.2	1.24	V	Enable PGO
		1.16	1.2	1.24	V	PGO/UVP Disable
	VHV2	0		50	mV	OP hysteresis voltage

FPOB, Open Drain Output:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leakage Current	Ileak			+/- 5	uA	VFPOB=12V
Low Level Output Voltage	VOL			0.5	V	ISINK=10mA

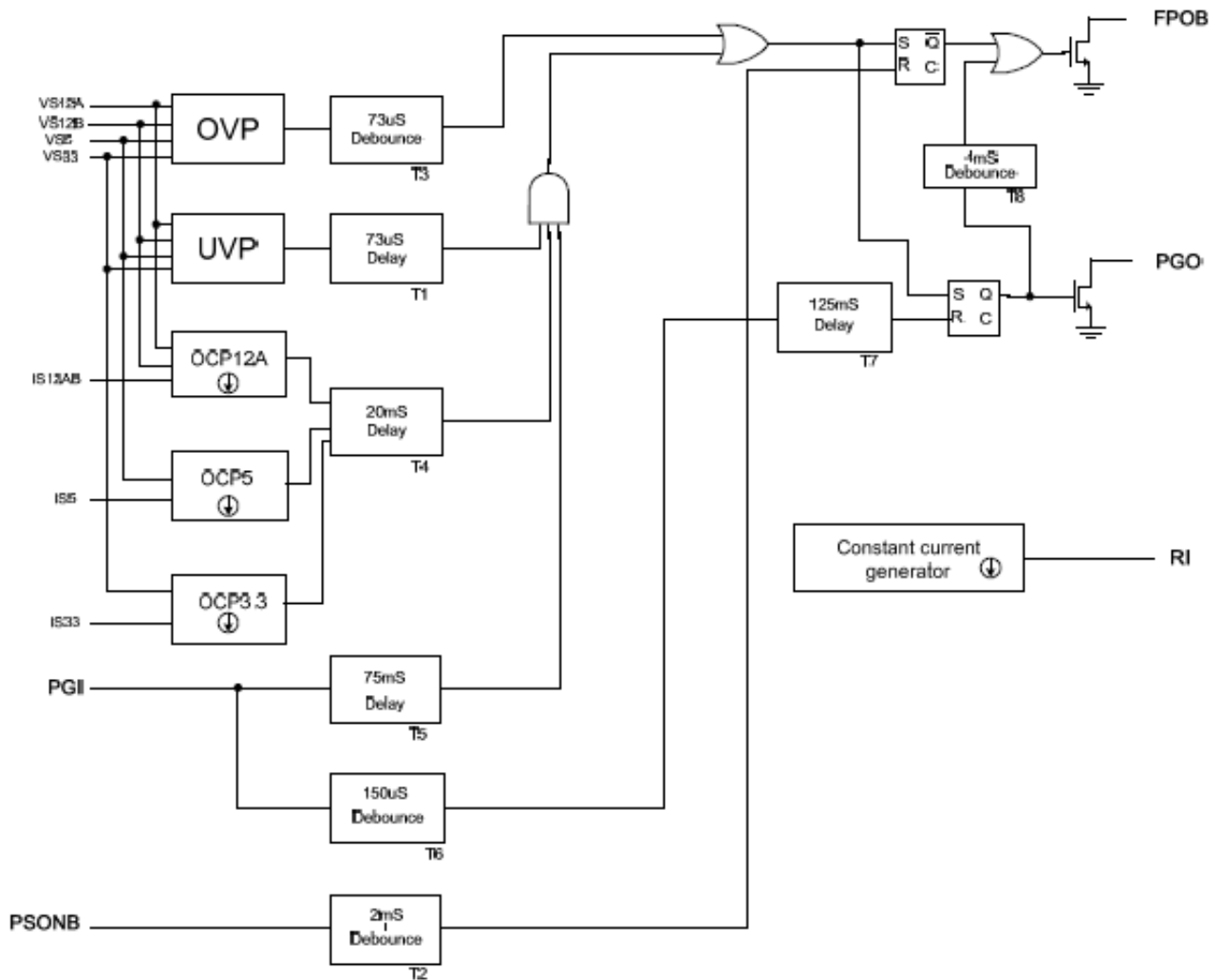
PGO, Open Drain Output:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leakage Current	Ileak			+/- 5	uA	VPGO=5V
Low Level Output Voltage	VOL			0.3	V	ISINK=20mA

AC Electrical Characteristics (Vcc=12V, Ta=25°C)

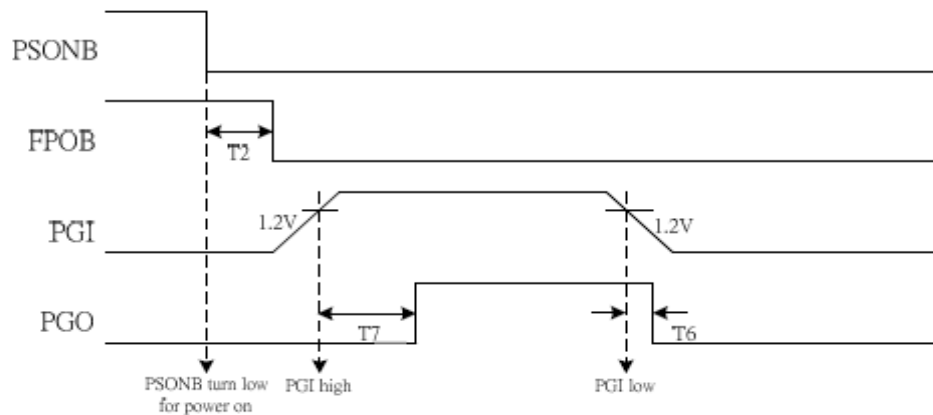
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Under voltage protection delay time	T1	49	73	100	uS	500 PPM/°C
PSON De-bounce time	T2	1	2	3	mS	
Over voltage protection delay time	T3	49	73	100	uS	
Over current delay time	T4	13	20	27	mS	
PGI OC/UV mask time	T5	49	75	100	uS	
PGO De-bounce time	T6	120	150	180	mS	
PGI to PGO delay time	T7	110	125	140	mS	
PGO to FPOB delay time	T8	2	4	6	mS	

Block Diagram

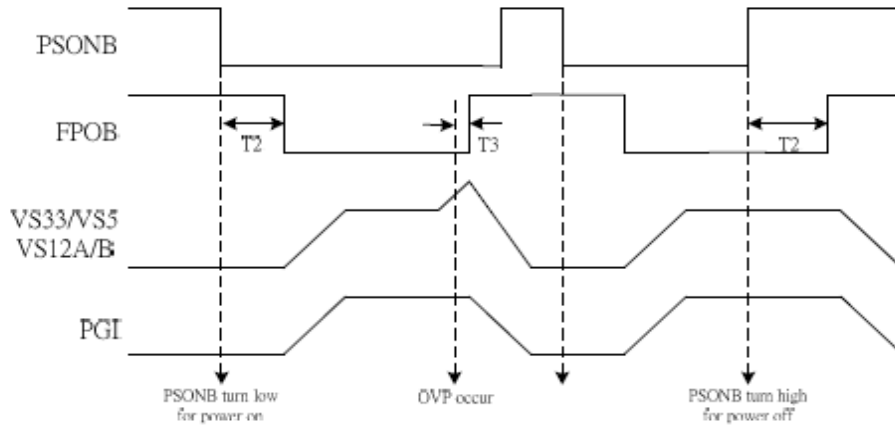


Time Chart

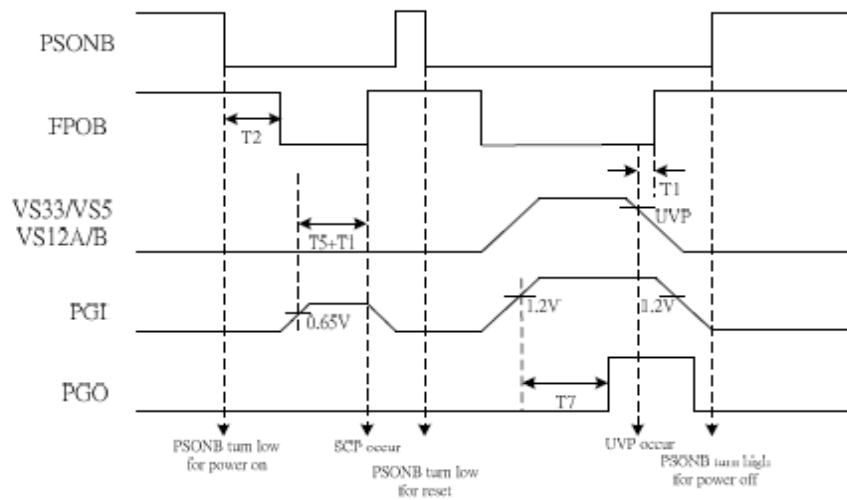
PGI Timing



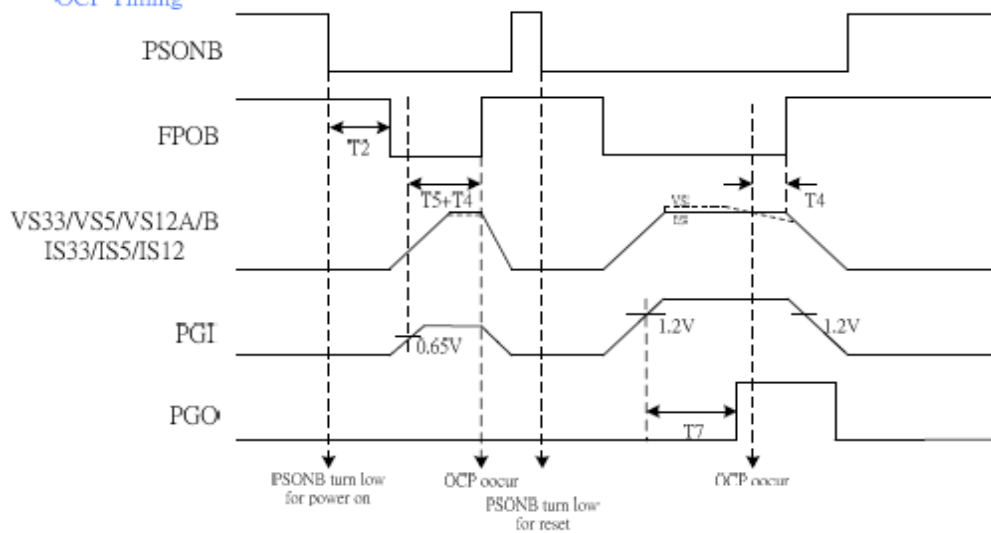
OVP Timing



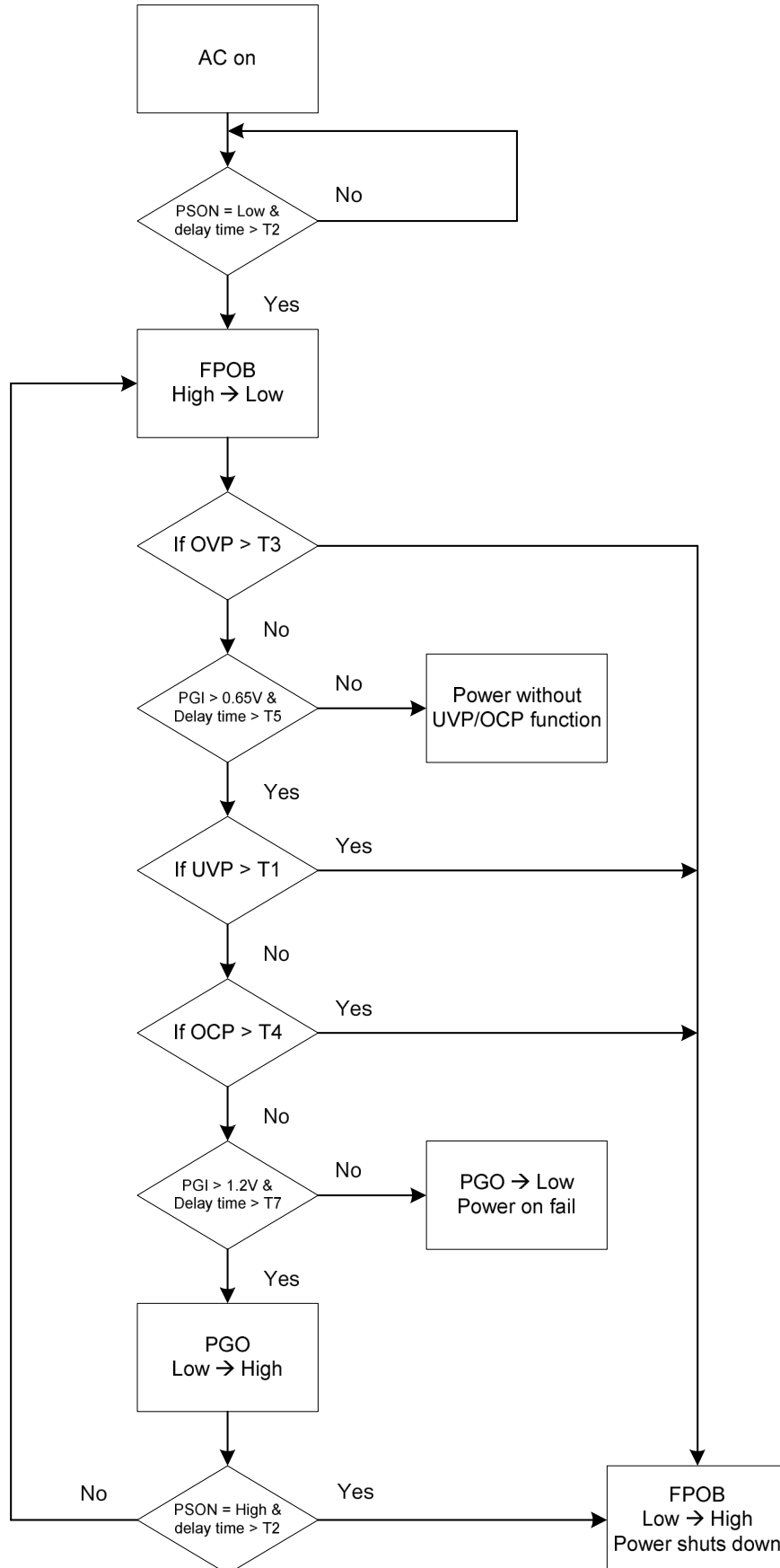
SCP & UVP Timing



OCP Timing



Flow Chart



Function & Application Descriptions

Pin-PGI:

Secondary detect point between flywheel diode and inductance. When AC on/off, PGI can control protection function when output voltages rise or fall to prevent the PSU malfunction.

- 1 Setting PGI voltage (range: 1.5V~2V) with resistance divider.
- 2 To suppress the PGI noise, user can use a capacitor (range: 0.1uF~1.0uF) between PGI and GND.
- 3 Exact OP switch point helps the PF time design easier.
- 4 PGI has three states (0.65V, 0.8V and 1.2V) control function. The state control function is described below:
 - 1) $V_{PGI} < 0.65V$:
The UVP and OCP functions are disabled.
 - 2) $0.65V < V_{PGI} < 1.2V$:
If UV/OC conditions are set, PGI triggers UVP after $T_5 + T_1$ and OCP after $T_5 + T_4$. If no fail conditions, PSU outputs work normally but without Power Good signal.
 - 3) $V_{PGI} > 1.2V$:
If UV/OC conditions are set before AC turn on, PGI triggers UVP after $T_5 + T_1$ and OCP after $T_5 + T_4$. If UV/OC conditions are set after AC turn on and delay T_5 , UVP triggered delay time is T_1 and OCP triggered delay time is T_4 . If no fail conditions, PSU outputs work normally and with Power Good signal.
 - 4) PGI function:
When $V_{PGI} < 1.2V$, the PG output signal and UVP is disabled. But OCP function is disabled when $V_{PGI} < 0.8V$.

Pin-PSON:

- a) An input control pin, through a remote on/off input signals to control the FPOB and PGO output pin states.
- b) A 2ms de-bounce built-in for rising and falling edge triggered control.
- c) PSON is also built-in a pulled high resistance to VDD inside to provide a high state control when pin is floating.
- d) TTL logic-compliant input voltage threshold with a hysteresis design.

Pin-VS/IS (VIS33/VIS5/VIS12):

The IC OCP function input pins. When pin-VS voltage is under pin-IS voltage, OCP functions and changes FPOB/PGO states. The pin-VS also provides the OVP and UVP functions. If pin-VS voltage is unstable and keeps a under voltage condition for T_1 or a over voltage condition for T_3 , the FPOB/PGO states will be changed.

- a) The anti-noise capacitor between VS and IS can suppress input noises and make more accurate OCP function.
- b) Due to high ESD performance, the VS series resistance or parallel capacitor can be ignored and indirectly reduce OCP function error.

Pin-RI:

A constant output voltage for building OCP reference current. Set a resistance (range: 15K Ω ~120K Ω) from RI to GND, The reference current equals to V_{RI} divided by resistance and pin-IS current is RI's 8 times.

Pin-FPOB/PGO:

The FPOB and PGO are both open-drain devices. If AC turns on and PSU outputs are normal, $V_{PGI} > 1.2V$ and delay T_7 continually, PGO state will keep at high through a resistance pulled to 5V output. Due to high ESD performance, the PGO series resistance can be ignored.

The FPOB is used to control the primary side PWM via an opto-coupler. A series resistance pulled to standby power is used to limit the opto-coupler and FPOB operation current. When IC is not ready or one of protect function is triggered, PSON keeps at high state, the level of FPOB is high and the PWM will shut down.

Function & Application Descriptions (Cont.)

How to set output current protection:

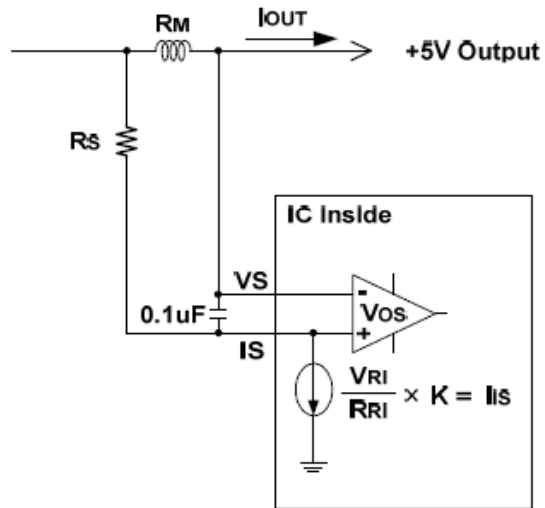
The parameters are IS pin sink current (IIS), IS pin series resistance (RS), Output resistance (RM) and OP offset voltage (VOS). For example, we want to set 5V output current "IOUT",

$$I_{OUT} \times R_M = I_{IS} \times R_S + V_{OS}$$

$$I_{OUT} = \frac{I_{IS} \times R_S + V_{OS}}{R_M}$$

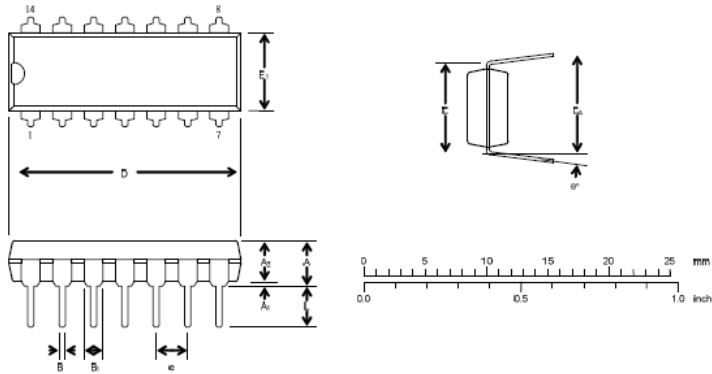
if $I_{IS}=160\mu A$, $V_{OS}=0mV$, $R_S=500\Omega$, $R_M=2m\Omega$

$$I_{OUT} = \frac{160\mu \times 500 + 0m}{2m} = 40A$$



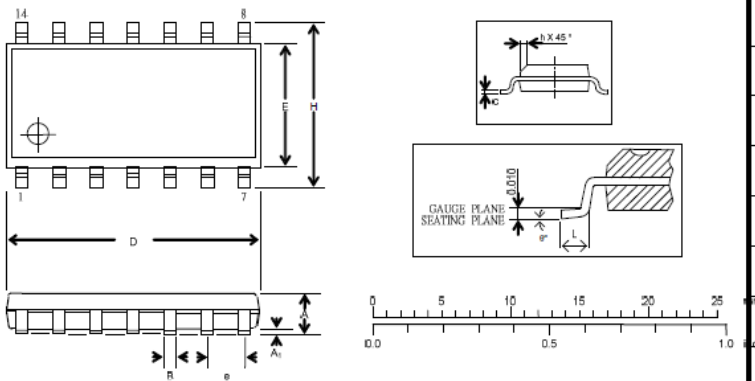
PACKAGING INFORMATION

DIP-14L



Symbol	Dimension in mm		Dimension in inch	
A	4.318	(MAX)	0.170	(MAX)
A ₁	0.381	(MIN)	0.015	(MIN)
A ₂	3.302	±0.127	0.130	±0.005
B	0.457	(TYP)	0.018	(TYP)
B ₁	1.524	(TYP)	0.060	(TYP)
D	19.101	± 0.127	0.752	± 0.005
E	7.620	± 0.254	0.300	± 0.010
E ₁	6.401	± 0.127	0.252	±0.005
e	2.540	(TYP)	0.100	(TYP)
E _A	9.017	± 0.508	0.355	± 0.020
L	3.302	± 0.254	0.130	±0.010
θ°	0° ~ 15°		0° ~ 15°	

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Symbol	Dimension in mm		Dimension in inch	
A	1.750	(MAX)	0.069	(MAX)
A ₁	0.100	0.25	0.004	0.01
B	0.330	0.51	0.013	0.02
C	0.100	0.25	0.004	0.010
e	1.270	(TYP)	0.050	(TYP)
D	8.650	(TYP)	0.340	(TYP)
H	6.000	(TYP)	0.236	(TYP)
E	3.900	(TYP)	0.154	(TYP)
L	0.400	1.27	0.016	0.05
h	0.250	0.50	0.010	0.020
θ°	0° ~ 8°		0° ~ 8°	