Data Sheet

Type Description: High-Voltage Resonant Half-Bridge Controller

Product Name: EST.9002A

Reversion: 1.10

Reversion Date: August 06, 2014

Page: 9 Pages

Issue Date: 2014/Aug/06

Description

The EST.9002A is a control IC specific for resonant half-bridge topology. It provides 50% complementary duty cycle signals of the high-side switch (HVG) and the low-side switch (LVG). And a fixed dead-time inserted between HVG and LVG transient guarantees soft-switching and enabled high-frequency operation.

The IC built-in a 600V high-voltage floating structure that drive the high-side switch with the bootstrap approach, an external fast-recovery bootstrap diode between VCC and VBOOT must be added.

Output voltage regulation is obtained by modulating the operating frequency. An externally programmable oscillator can set the operating frequency range of the converter.

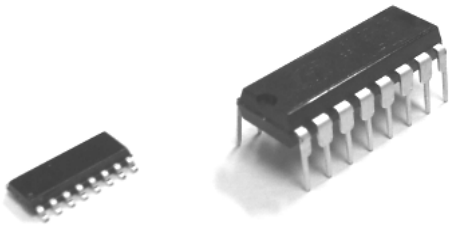
As start-up, to prevent uncontrolled inrush current, the switching frequency starts from a programmable maximum value and progressively decays until it reaches the steady-state value determined by the control loop. This frequency shift is non linear to minimize output voltage overshoots; its duration is programmable as well.

At light load the IC may enter a controlled burst-mode operation that keeps the converter input consumption to a minimum.

IC's functions include a not-latched active-low disable input (LINE) with current hysteresis useful for power sequencing or for brownout protection, a current sense (ISEN) for OCP with frequency shift and delayed shutdown with automatic restart. A higher level OCP latched off the IC if the first-level protection is not sufficient to control the primary current. Their combination offers complete protection against overload and short circuits. An additional latched disable input (DIS) allows easy implementation of OTP and/or OVP.

An interface with the PFC controller is provided that enables to switch off the pre-regulator during fault conditions, such as OCP shutdown and DIS high, or during burst-mode operation.

Package



SOP-16L DIP-16L

Applications

- LCD and PDP TV
- Desktop PC and Server
- Telecom SMPS
- Industrial SMPS
- AC-DC Adapter, open frame SMPS

Features

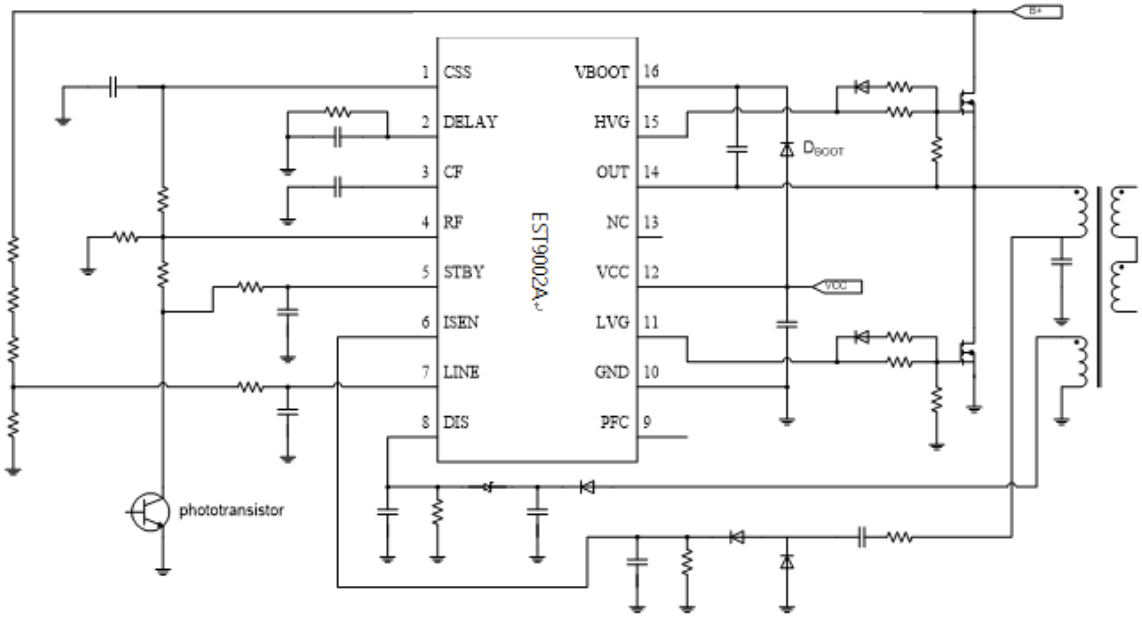
- 50% duty cycle, variable frequency control of resonant half-bridge converter
- High-accuracy oscillator
- Up to 500KHz operating frequency
- Two-level OCP : frequency-shift and latched shutdown
- Interface with PFC controller
- Latched disable input
- Burst-mode operation at light load
- Input for power-ON/OFF sequencing or brownout protection
- Non-linear soft-start for monotonic output voltage rise
- -300mA / 800mA peak current for high-side and low-side gate drivers
- Built-in 600V high-voltage floating high-side gate driver
- The external fast-recovery bootstrap diode between VCC and VBOOT must be added

ORDERING INFORMATION

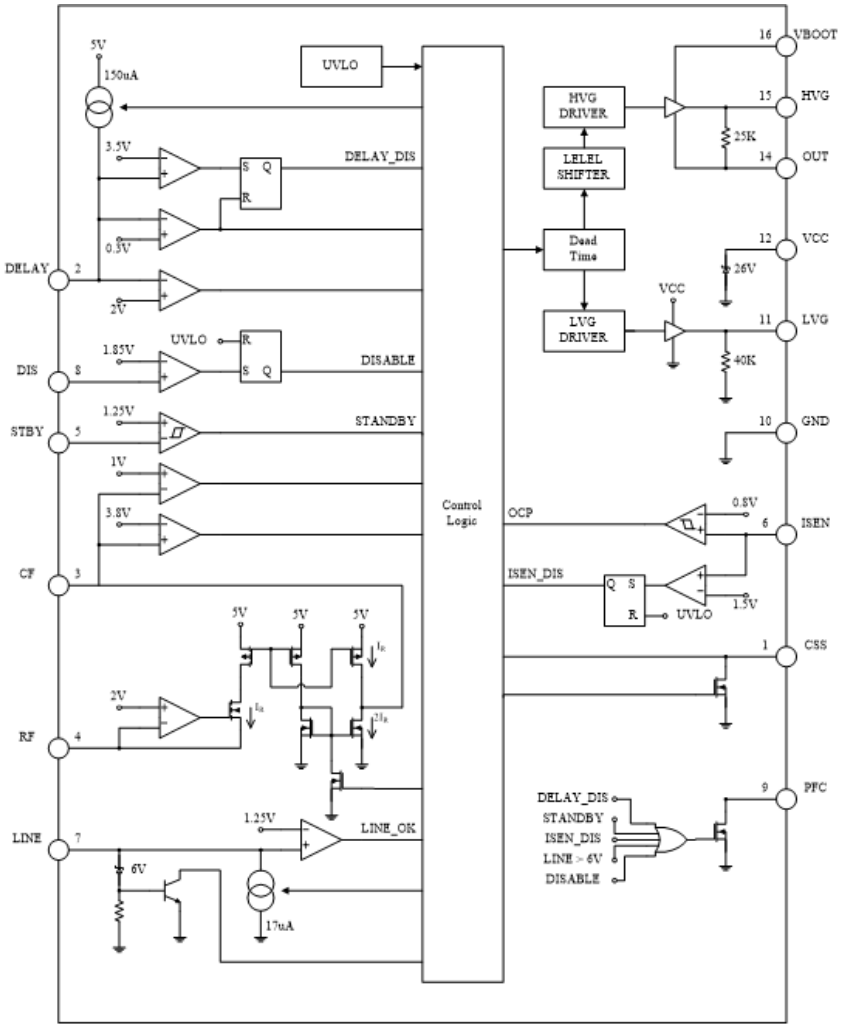
ORDER NUMBER	Package	Shipping	Top Marking
EST9002AD	DIP-16(Pb-free)	Tube	EST9002AD
EST9002AS	SOP-16(Pb-free)	Tube	EST9002AS
EST9002ASR	SOP-16(Pb-free)	Tape & Reel	EST9002AS

Typical Application Circuit

■ **The external fast-recovery bootstrap diode (DBOOT) between VCC and VBOOT must be added.**



Block Diagram



Pin Description

Pin Functions

Pin	Symbol	Function
1	CSS	***Soft-start.*** This pin connects a capacitor to GND and a resistor to RF pin that set both the oscillator frequency and the time constant of the frequency shift during soft-start. An internal switch discharges the capacitor during the IC turns off (VCC < UVLO, LINE < 1.25V, LINE > 7V, DIS > 1.85V, ISEN > 1.5V, ISEN > 0.8V as long as it stays above 0.75V or DELAY > 2V) to make sure it will be soft-started next.
2	DELAY	***Delay time for over-current.*** This pin connects a capacitor and a resistor to GND that set both the de-bounce time of an over-current condition and the auto-restart time. When the ISEN voltage exceeds 0.8V, the capacitor is charged by an internal current 150uA and is slowly discharged by the external resistor. When the DELAY voltage reaches 2V, both the 150uA and the CSS switch is kept always on. When the DELAY voltage exceeds 3.5V, the IC stops switching and the 150uA turned off, then the DELAY voltage will decay by the external resistor. Until the DELAY voltage drops below 0.3V, the IC will be soft-started again. $T_{OC} \approx 100ms \ldots C_{DELAY} = 1uF$ $T_{SD} = \frac{3.5V - 2V}{150uA} C_{DELAY} \approx 10^4 C_{DELAY}$ $T_{RESTART} = R_{DELAY} C_{DELAY} \ln \frac{3.5V}{0.3V} \approx 2.5 R_{DELAY} C_{DELAY}$
3	CF	***Oscillator capacitor.*** This pin connects a capacitor to GND that set the switching frequency by a programmed current of the external network connected to RF pin.
4	RF	***Oscillator resistor.*** This pin provides a reference voltage 2V and a programmed current by the external resistor. First, this pin connects a resistor to GND defines a minimum current that is used to set the minimum oscillator frequency. Second, this pin connects a resistor to phototransistor that regulates the converter output voltage by modulating the oscillator frequency. Third, this pin connects a resistor to CSS pin that set soft-start and over-current oscillator frequency. $Freq = \frac{1}{2.8 \times C_{CF} \times R_{RF}}$
5	STBY	***Burst-mode input.*** This pin provides burst-mode operation during no or very light load by sensing voltage related to the feedback control. When the STBY voltage goes below 1.25V, the IC enters an idle state. Until the STBY voltage exceeds 1.3V then the IC restarts switching and soft-start is not invoked. Tie the STBY to RF pin if burst-mode function is not used.
6	ISEN	***Over-current sense input.*** This pin senses the primary current though a sense resistor or a capacitive divider for lossless sensing. The ISEN voltage must be filtered to get average current information, it is not for a cycle-by-cycle control. If the ISEN voltage exceeds 0.8V (with 50mV hysteresis), the CSS

		switch is pulled to GND and the DELAY current turned on. If the ISEN voltage exceeds 1.5V, the IC is latched shutdown and the latch state is removed during UVLO. Tie the ISEN pin to GND if the function is not used.
7	LINE	***Line sense input.*** This pin connects an external resistor divider from the high-voltage input bus that set the brownout voltage. When the LINE voltage goes below 1.25V, the IC turns off and an internal sink current 17uA is ON. When the LINE voltage is clamped to about 7V by an internal zener, the IC turns off. This pin connects an external bypass capacitor to GND to reduce noise pick-up. Bias the LINE between 1.25V and 6V if the function is not used. $R_H = \frac{Vin_{ON} - Vin_{OFF}}{17uA}$ $R_L = R_H \frac{1.25V}{Vin_{OFF} - 1.25V}$
8	DIS	***Latched shutdown input.*** When the DIS voltage exceeds 1.85V, the IC is latched shutdown and the latch state is removed during UVLO. Tie the DIS to GND if the function is not used.
9	PFC	***Open-drain output for PFC controller.*** This pin, normally open, is intended for stopping the PFC controller, during protection or burst-mode. The PFC is pulled low every time the IC turns off (LINE > 7V, DIS > 1.85V, ISEN > 1.5V, DELAY > 2.0V as long as it stays above 0.3V or STBY < 1.25V). The PFC is open during UVLO to let the PFC controller start first. The PFC is open during LINE < 1.25V to reduce the IC's consumption. Leave the PFC unconnected if the function is not used.
10	GND	***IC ground.***
11	LVG	***Low-side gate-drive output.*** This pin used to drive the lower MOSFET of the half-bridge leg. The LVG is pulled to GND during UVLO.
12	VCC	***IC Supply voltage.*** This pin connects an external bypass capacitor to GND.
13	NC	***High-voltage spacer.***
14	OUT	***High-side gate-drive floating ground.***
15	HVG	***High-side gate-drive floating output.*** This pin used to drive the upper MOSFET of the half-bridge leg. This pin connects an internally resistor to OUT pin that ensures the HVG is not floating during UVLO.
16	VBOOT	***High-side gate-drive floating supply voltage.*** This pin connects an external bootstrap capacitor to OUT pin that is fed by an external bootstrap diode.

Absolute Maximum Ratings

Symbol	Pin	Parameter	Min.	Max.	Units
VBOOT, OUT	16, 14	Floating Supply Voltage	-0.3	18	V
HVG	15	Floating Output Voltage	OUT-0.3	VBOOT+0.3	V
OUT	14	Floating Ground Voltage	-3	600	V
		Floating Ground Maximum Slew Rate	-	50	V/ns
VCC	12	IC Supply Voltage	-0.3	18	V
LVG	11	Output Voltage	-0.3	VCC+0.3	V
PFC	9	Output Voltage	-0.3	30	V
LINE	7	Clamp Voltage (Current = 1mA)	-	8	V
RF	4	Source Current	-	2	mA
STBY, ISEN, DIS	5, 6, 8	Input Voltage	-0.3	7	V
		Power Dissipation at T_A=70℃ (PDIP-16)	-	1	W
		Power Dissipation at T_A=50℃ (SOP-16)	-	0.83	W
		Operating Junction Temperature	-40	150	℃
		Storage Temperature	-55	150	℃
		Soldering Temperature	-	260	℃

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Thermal Data

Symbol	Parameter	Value	Units
θ_{JA}	Maximum thermal resistance from junction to ambient (PDIP-16)	80	℃/W
	Maximum thermal resistance from junction to ambient (SOP-16)	120	℃/W

Electrical Characteristics

T_J =0 to 105℃, VCC =15V, VBOOT = 15V, OUT = 0V, C_{HVG}=C_{LVG}=1nF, C_{CF} = 470pF, R_{RF}=12KΩ; unless otherwise specified.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
VCC Supply Voltage						
VCC	VCC Operating Voltage	After IC turn on	8.7	-	16	V
VCC_{ON}	VCC Turn On Threshold	Voltage rising	10.0	10.7	11.4	V
VCC_{OFF}	VCC Turn Off Threshold	Voltage falling	7.3	8.0	8.7	V
VCC_{CLAMP}	VCC Clamp Voltage	Clamp current = 15mA	22	26	30	V
VCC Supply Current						
ICC_{OFF}	VCC Start Current	VCC = 10V before IC turn on	-	650	900	uA
$ICC_{STANDBY}$	VCC Standby Current	STBY = 1V	-	1.7	2.4	mA
$ICC_{OPERATE}$	VCC Operating Current	STBY = 2V	-	5.5	7.7	mA
VBOOT High-side Gate-drive Floating Supply Voltage						
$I_{LK-VBOOT}$	VBOOT Leakage Current	VBOOT = 580V	-	-	10	uA
I_{LK-OUT}	OUT Leakage Current	OUT = 562V	-	-	10	uA
ISEN Over Current Sense						
$I_{LK-ISEN}$	ISEN Leakage Current	ISEN = 0V to 5V	-1	-	1	uA
$V_{TH-ISEN}$	ISEN Threshold	Voltage rising	0.75	0.8	0.85	V
$V_{HYS-ISEN}$	ISEN Hysteresis Window	Voltage falling	-	50	-	mV
$V_{LATCH-ISEN}$	ISEN Latch Shutdown Threshold	Voltage rising	1.45	1.5	1.55	V
Delay Over Current Function						
$I_{LK-DELAY}$	DELAY Leakage Current	DELAY = 1V, ISEN = 0V	-1	-	1	uA
$I_{CHARGE-DELAY}$	DELAY Charge Current	DELAY = 1V, ISEN = 1V	100	150	200	uA
$V_{OC-DELAY}$	DELAY Threshold for Over Current	Voltage rising	1.9	2.0	2.1	V
$V_{SD-DELAY}$	DELAY Threshold for Shutdown	Voltage rising	3.3	3.5	3.7	V
$V_{RESTART-DELAY}$	DELAY Threshold for Restart	Voltage falling	0.25	0.3	0.35	V

Electrical Characteristics

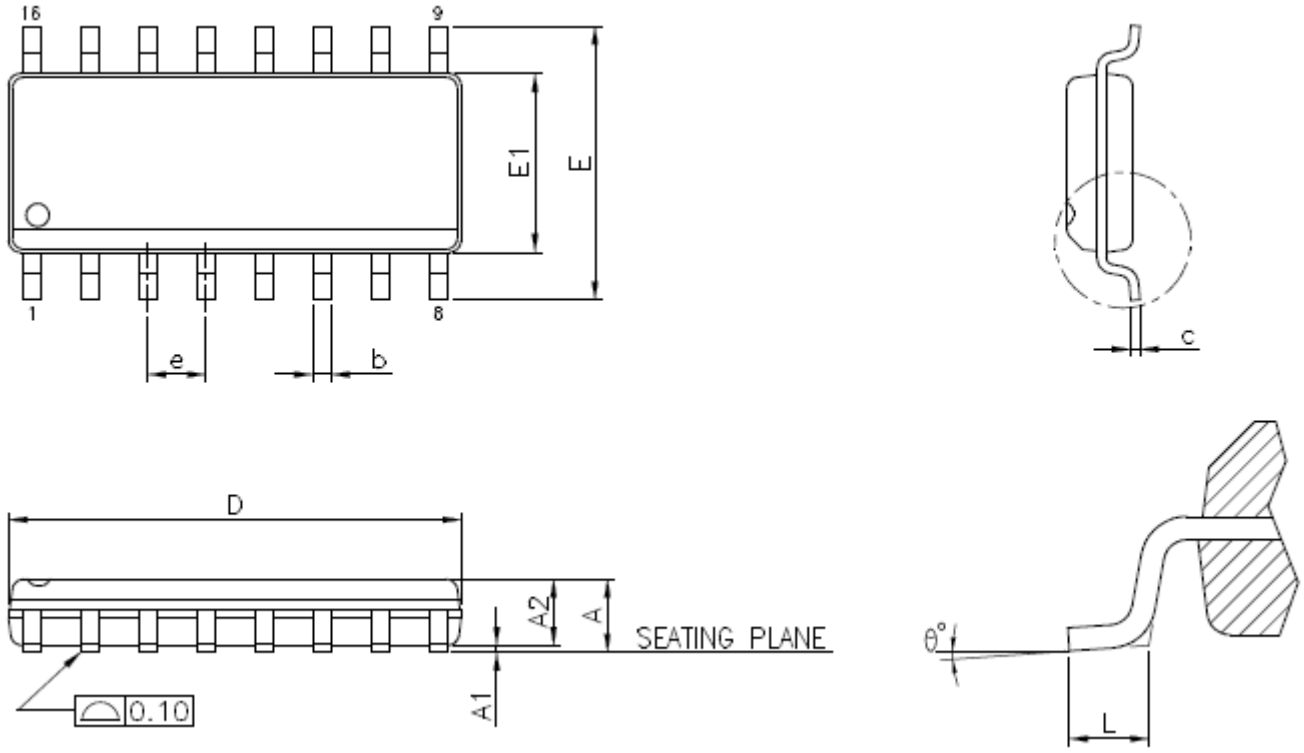
T_J =0 to 105℃, VCC =15V, VBOOT = 15V, OUT = 0V, C_{HVG}=C_{LVG}=1nF, C_{CF} = 470pF, R_{RF}=12KΩ; unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Line Sense						
$V_{TH-LINE}$	LINE Threshold	Voltage rising or falling	1.2	1.25	1.3	V
$I_{SINK-LINE}$	LINE Sink Current	LINE = 1.1V	12	17	22	uA
$V_{CLAMP-LINE}$	LINE Clamp Voltage	Clamp current = 1mA	6	-	8	V
DIS Function						
I_{LK-DIS}	DIS Leakage Current	DIS = 0V to 5V	-1	-	1	uA
V_{TH-DIS}	DIS Threshold	Voltage rising	1.78	1.85	1.92	V
PFC Output						
I_{LK-PFC}	PFC Leakage Current	PFC = 0V to VCC	-1	-	1	uA
$I_{SINK-PFC}$	PFC Sink Current	PFC = 0.2V, STBY = 0V	1	-	-	mA
CSS Soft-start Function						
I_{LK-CSS}	CSS Leakage Current	CSS = 0V to 5V	-1	-	1	uA
$I_{SINK-CSS}$	CSS Sink Current	CSS = 0.2V, LINE = 0V	1	-	-	mA
STBY Burst Mode Function						
$I_{LK-STBY}$	STBY Leakage Current	STBY = 0V to 5V	-1	-	1	uA
$V_{TH-STBY}$	STBY Threshold	Voltage falling	1.2	1.25	1.3	V

$V_{HYS-STBY}$	STBY Hysteresis Window	Voltage rising	-	50	-	mV
Oscillator						
V_{REF-RF}	RF Reference Voltage	R_{RF} = 1KΩ or 12KΩ	1.93	2	2.07	V
F_{OSC}	Oscillation Frequency	R_{RF} = 12KΩ	60.6	62.5	64.4	KHz
		R_{RF} = 2.7KΩ	245	255	265	
Duty	Duty Cycle of LVG and HVG		48	50	52	%
T_{DEAD}	Dead Time between HVG and LVG		0.3	0.4	0.5	us
t_{LEB}	Leading Edge Blanking	After positive edge of HVG and LVG	-	250	-	ns
LVG Low-side Gate Driver Output						
$I_{SINK-LVG}$	LVG Sink Current	LVG = 1.5V	200	-	-	mA
$I_{SOURCE-LVG}$	LVG Source Current	LVG = 12.8V	5	-	-	mA
$I_{PK-SOURCE}$	LVG Peak Source Current		-0.3	-	-	A
$I_{PK-SINK}$	LVG Peak Sink Current		0.8	-	-	A
t_{F-LVG}	LVG Falling Time		-	30	-	ns
t_{R-LVG}	LVG Rising Time		-	60	-	ns
	LVG Pull-down Resistor to GND		-	40	-	KΩ
HVG High-side Gate Driver						
$I_{SINK-HVG}$	HVG Sink Current	HVG = 1.5V	200	-	-	mA
$I_{SOURCE-HVG}$	HVG Source Current	HVG = 12.8V	5	-	-	mA
$I_{PK-SOURCE}$	HVG Peak Source Current		-0.3	-	-	A
$I_{PK-SINK}$	HVG Peak Sink Current		0.8	-	-	A
t_{F-HVG}	HVG Falling Time		-	30	-	ns
t_{R-HVG}	HVG Rising Time		-	60	-	ns
	HVG Pull-down Resistor to OUT		-	25	-	KΩ

Package Outlines Dimensions

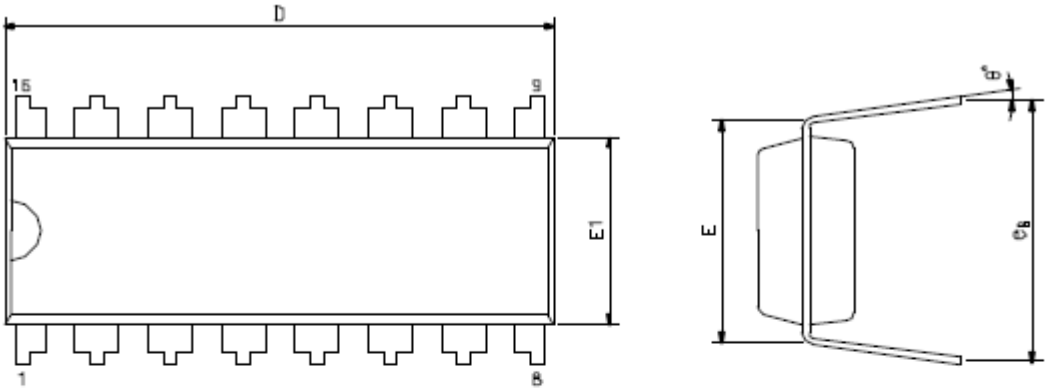
SOP-16 Small Outline Package

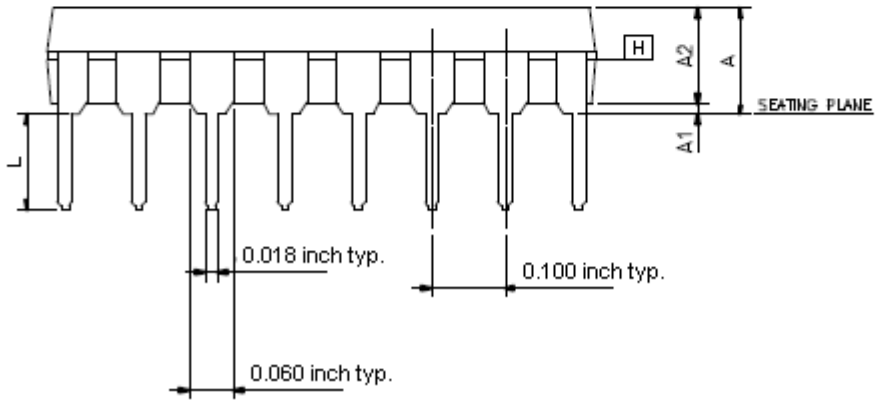


Symbols	Dimensions In inch		Dimensions In millimeters	
	Min.	Max.	Min.	Max.
A	------	0.072	------	1.837
A1	0.004	0.010	0.095	0.263
A2	0.047	------	1.187	------
b	0.012	0.021	0.294	0.535
c	0.004	0.010	0.095	0.263
D	0.390 BSC		9.900 BSC	
E	0.236 BSC		6.000 BSC	
E1	0.154 BSC		3.900 BSC	
e	0.050 BSC		1.270 BSC	
L	0.015	0.052	0.380	1.333
θ	0°	8°	0°	8°

Package Outlines Dimensions (continued)

PDIP-16 Plastic Dual In-line Package





Symbols	Dimensions in inches			Dimensions in millimeters		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	---	---	0.215	---	---	5.461
A1	0.010	---	---	0.254	---	---
A2	0.120	0.133	0.145	3.048	3.378	3.683
D	0.730	0.755	0.780	18.542	19.177	19.812
E	0.300 BSC			7.620 BSC		
E1	0.240	0.253	0.265	6.096	6.426	6.731
L	0.110	0.133	0.155	2.794	3.378	3.937
eB	0.300	0.350	0.430	7.620	8.890	10.922
θ	0°	7°	15°	0°	7°	15°

Update History

Revision	Date	Update
1.00	July 15, 2014	Preliminary version
1.10	August 06, 2014	Description , Features , Block Diagram , Pin Functions , Electrical Characteristics