Data Sheet

Type Description : 1–Channels Secondary Supervisor IC

Product Name : EST.7316/7316S

Reversion : Rev 1.0

Reversion Date : 01, 2020

Page : 18 Pages

Description

EST.7316 is higher integrated circuit incorporates all advance sensing function to protect from over and under voltage a three-channe protection supervisor (Triple 12V).

EST.7316 over current protection (OCP) monitors output currents b using smart comparator circuit to make the point setting through sens resistor is more exact and easy.

EST.7316 provides the fault protection latch (FPOB), a power goc output (PGO), the PSONB control and a power good input control p (PGI).

Features

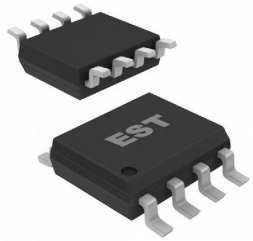
- The Over/Under Voltage Protection for 12V.
- The Over Current Protection monitors 12V output currents and related lockout
- Both of fault protection output and power good output are open drain output stage
- 40ms delay for SPS short circuit protect
- 46ms for PSONB input signal de-bounce
- 35us for OVP delay time
- 55us for UVP delay time
- 25ms for OCP delay time
- 73us for internal noise immunity de-bounce
- 300ms power good delay time for PGO
- 3.5ms time delay between PGO and FPOB when PSONB turns high

Application

- PC SPS line housekeeping IC

Pin Assignments

DIP-8L

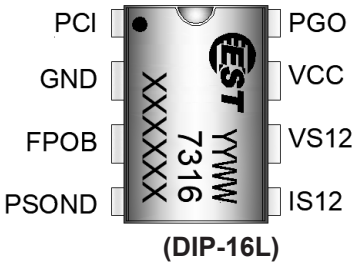


SOP-8L

Ordering Information

Order Number	Package Type	Packing	Top Marking
EST7316	DIP-8 (RoHS)	Tube	EST.7316
EST7316S	SOP-8 (RoHS)	Tube	EST.7316S
EST7316SR	SOP-8 (RoHS)	Tape & Reel	EST.7316S

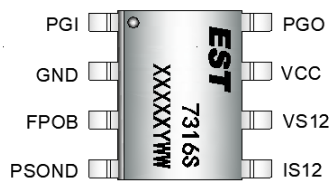
Pin connection (Top View)



(DIP-16L)

EST: LOGO
7316 : Product name DIP

YYWW: Date Code
XXXXXX: Production lot



(SOP-16L)

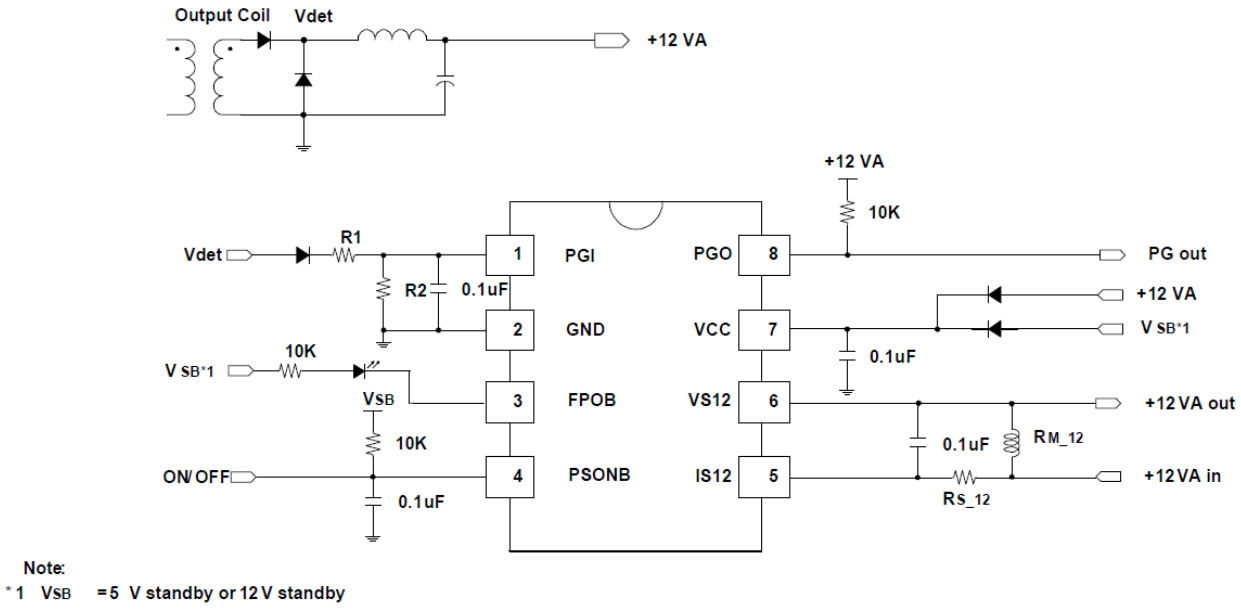
EST: LOGO
7316S= Product name SMD

XXXXYWW:
XXXX: Production lot
YWW: Date Code

Pin Description

Designation	No.	I/O	Description
PGI	1	I	Power good signal & UVP / OCP / VX input control pin.
GND	2	-	Ground.
FPOB	3	O	Inverted fault protection output pin. Open drain output stage.
PSONB	4	I	Remote ON/OFF switch input control pin.
IS12	5	I	12V over current protection sense input pin.
VS12	6	I	12V over/under voltage protection input pin.
VCC	7	I	Power supply input pin.
PGO	8	O	Power good output stage pin.

Typical Application Circuit



Note:
*1 VSB =5 V standby or 12 V standby

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage Temperature (Tstg)	---	-55 to 150	℃
Operating Temperature (Topr)	---	-40 to 125	℃
Junction Temperature (Tj)	---	150	℃
Supply Voltage (VCC)	VCC	-0.5 to 20	V
Input Voltage Range (VI)	VS12, IS12, PGI,PSONB,	-0.5 to 20	V
Output Voltage Range (VO)	FPOB, PGO	-0.5 to 20	V
Power Dissipation	PD	800	mW
Thermal Resistance	θJA	85/DIP; 150/SOP	℃/W
ESD	V_{ESD}	Class3	/W

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	3.5	12	18	V	
Input Voltage Range	VS12, IS12, PGI, PSONB			16	V	
Output Voltage Range	FPOB, PGO, RI			16	V	

DC Electrical Characteristics (VCC =12V, Ta=25)

Input Power Supply:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	4	12	15	V	
Supply Current	Icc		1	1.5	mA	
Reset Threshold Voltage	VIH	2.8	3.0	3.2	V	HIGH→LOW*1

Over-Voltage function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Over-Voltage Threshold	OVT_{VS5}	13.40	13.70	14.00	V	
	OVT_{VS12}	13.30		14.14	V	Ta= -10℃~75℃

Under-Voltage function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Under-Voltage Threshold	UVT_{VS5}	9.50	10.00	10.50	V	
	UVT_{VS12}	9.44		10.62	V	Ta= -10℃~75℃

Over-Current function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Offset Voltage	V_{OS12A}	-2.0	0	2.0	mV	Offset voltage between I12 and V12
IS pin sink current	I_{Ssink}	156.0	160.0	164.0	uA	Ta= -10℃
		154.5		165.5		Ta= -10℃~75℃

PSONB, Analog Input function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pull-up current	V_{THH}		1.50		uV	PSON=0V
Threshold Voltage	V_{THL}	1.9			V	LOW→HIGH
Threshold Voltage	V_{THH}			1.10	V	HIGH→LOW

PGI, Analog Input function:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Temperature coefficient
Threshold Voltage of PGI	V_{PGI}	0.75	0.80	0.85	V	Enable UVP/OCP
		0.72		0.88		Ta= -10℃~75℃
		1.176	1.20	1.224	V	Disable UVP/OCP/PGO
		1.15		1.25		Ta= -10℃~75℃

FPOB, Open Drain Output:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leakage Current	I_{leak}			+/- 5	uA	V_{FPOB}=12V
Low Level Output Voltage	V_{OL}			0.3	V	I_{SINK}=5mA
				0.6	V	I_{SINK}=10mA

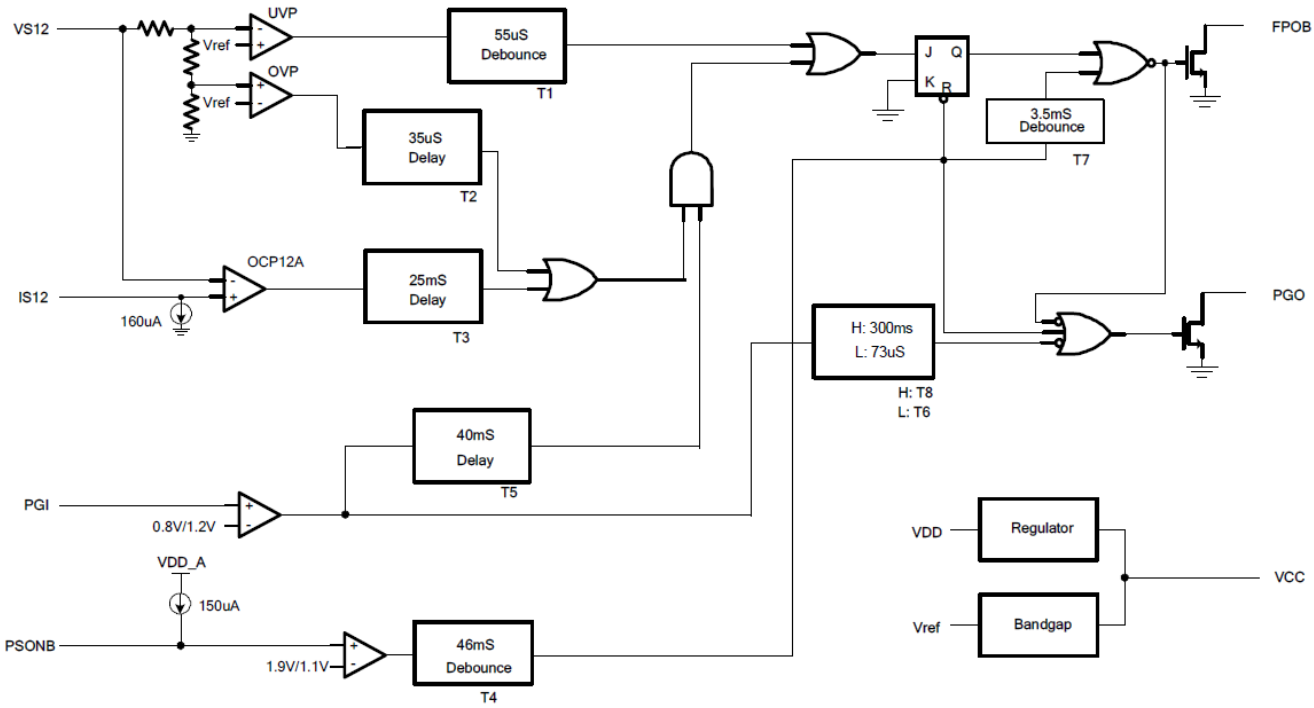
PGO (High level is into burst mode):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leakage Current	Ileak			+/- 5	uA	V_{PGO}=12V
Low Level Output Voltage	VOL			0.4	V	I_{SINK}=10mA

AC Electrical Characteristics (Vcc=12V, Ta=25℃)

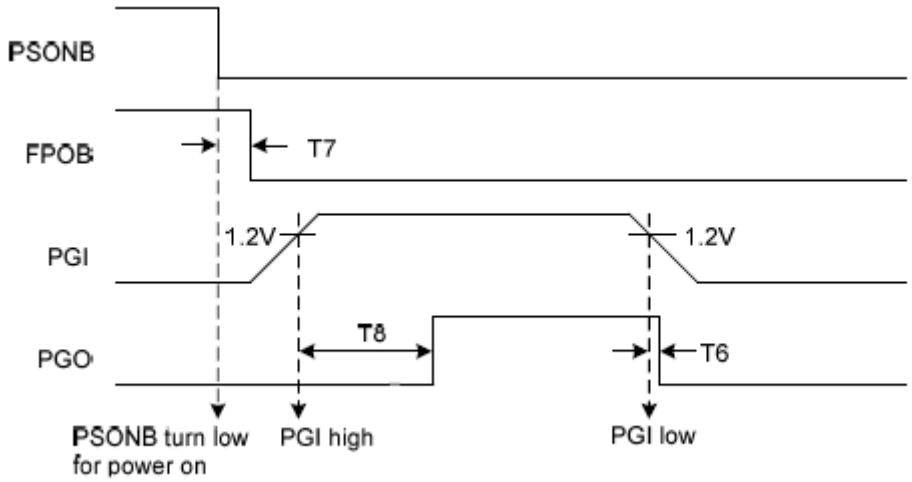
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Under Voltage Protection delay time	T1	35	55	75	uS	
Over Voltage Protection delay time	T2	20	35	50	uS	
Over Current Protection delay time	T3	20	25	30	mS	
PSONB De-bounce time	T4	32	46	61	mS	
PGI mask OCP/UVP delay time	T5	35	40	45	mS	PGI > 0.8V
PGI De-glitch time	T6	53	73	120	uS	PGI < 1.2V
PSONB to FPOB delay time	T7	T_4+2	T_4+3.5	T_4+5	mS	PSONB > 1.8V
PGI to PGO delay time	T8	250	300	350	mS	PGI > 1.2V

Block Diagram

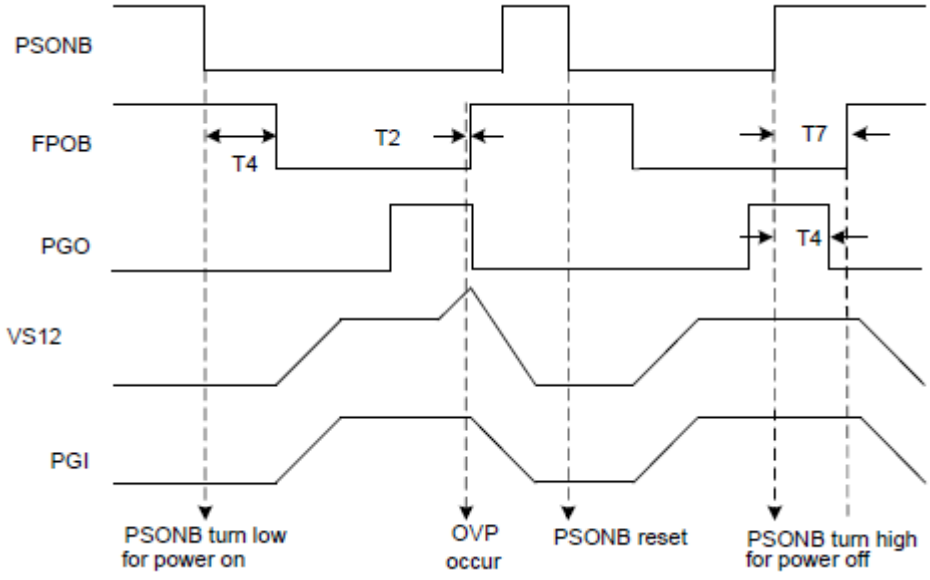


Time Chart

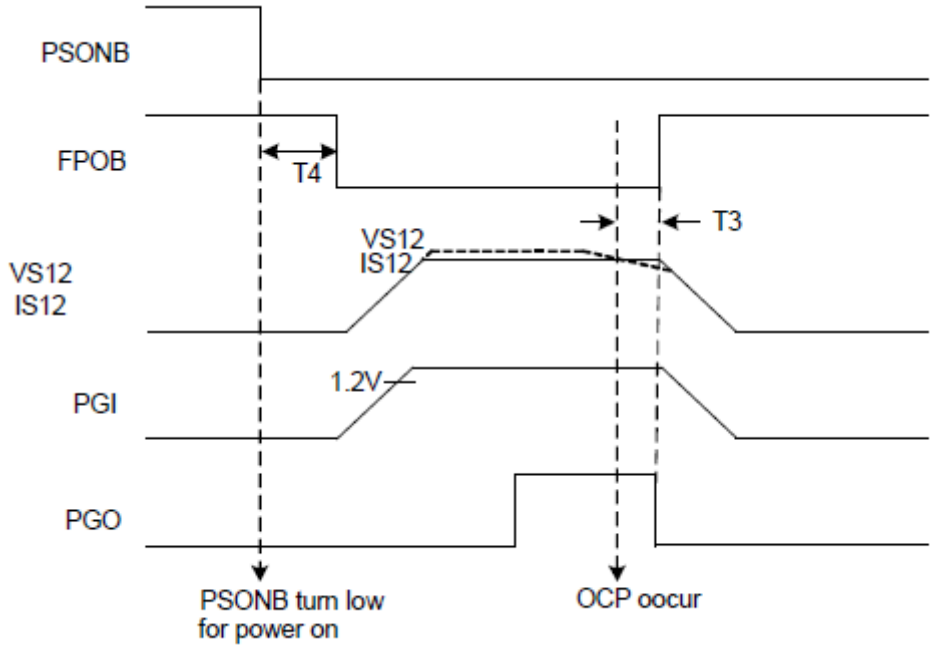
PGI Timing



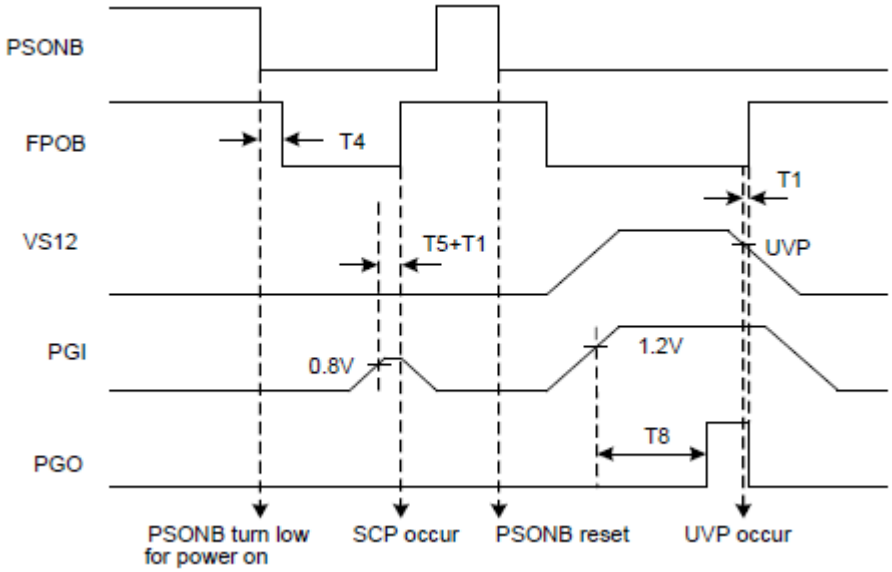
UVP Timing



OCP Timing

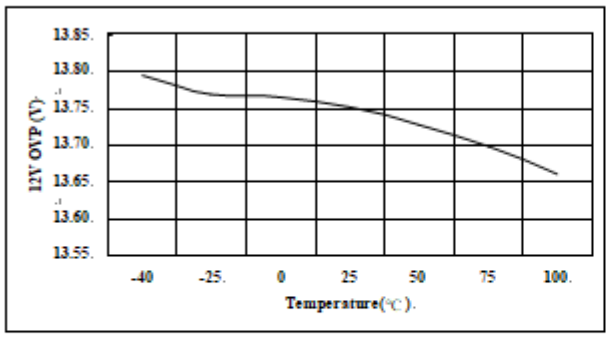


SCP & UVP Timing

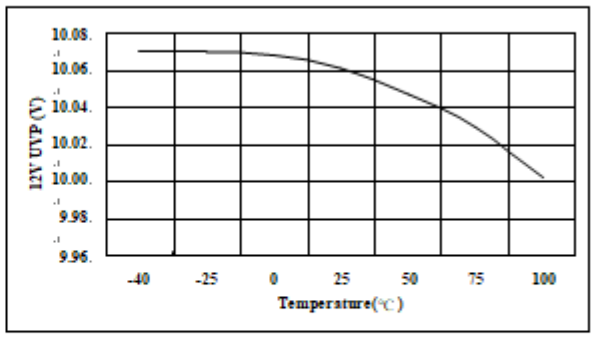


Typical Characteristic Temperature Curves

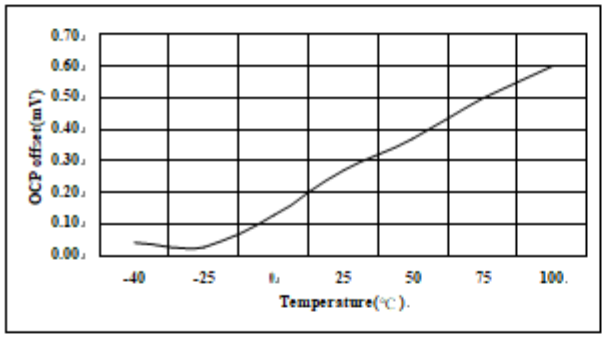
12V OVP vs. Temperature



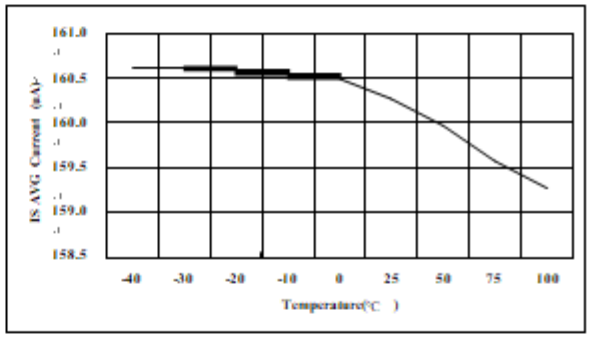
12V UVP vs. Temperature



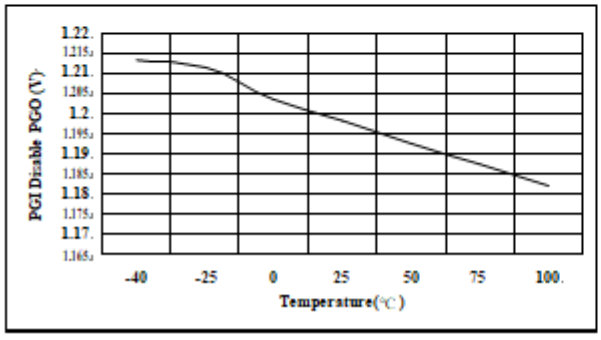
OCP offset vs. Temperature



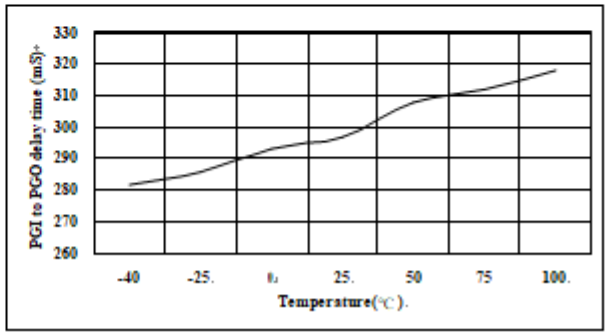
I12 Sink Current vs. Temperature



PGI Disable PGO Voltage vs. Temperature



PGI to PGO Delay Time vs. Temperature



Function & Application Descriptions

Pin-PGI:

Secondary detect point between flywheel diode and inductance. When AC on/off, PGI can control protection function when output voltages rise or fall to prevent the PSU malfunction.

a) Setting PGI voltage (range: 1.5V~2V) with resistance divider.
b) To suppress the PGI noise, user can use a capacitor (range: 0.1uF~1.0uF) between PGI and GND.
c) Exact OP switch point helps the PF time design easier.
d) PGI has two states (0.8V and 1.2V) control function. The state control function is described below:
   1) VPGI < 0.8V:
   2) The UVP and OCP functions are disabled. 2) 0.8V < VPGI < 1.2V:
   3) If UV/OC conditions are set before AC turn on, PGI triggers UVP after T5 + T1 and OCP after T5 + T3. If no fail conditions, PSU outputs work normally but without Power Good signal.
   4) If VPGI voltage larger then 1.2V at AC turn on, then VPGI voltage down to between 0.8V and 1.2V, the PSU will work normally because of the UVP/OCP functions are disabled.
   5) 3) VPGI > 1.2V:
   6) If UV/OC conditions are set before AC turn on, PGI triggers UVP after T5 + T1 and OCP after T5 + T3. If no fail conditions, PSU outputs work normally and with Power Good signal. If UV/OC conditions are set after AC turn on and delay T5, UVP will be triggered after T1 and OCP will be triggered after T3.

Pin-PSONB:

An input control pin, through a remote on/off input signals to control the FPOB and PGO output pin states.

a) A 46ms de-bounce built-in for rising and falling edge triggered control.
b) PSONB is also built-in a pulled high current source from VDD and to provide a high state control when pin is floated.
c) TTL logic-compliant input voltage threshold with a hysteresis design. The hysteresis is over 300mV.

Pin-VS12/IS12 :

The IC OCP function input pins. When pin-VS12 voltage is under pin-IS12 voltage, OCP functions and changes FPOB/PGO states. The pin-VS12 also provides the OVP and UVP functions. If pin-V12S voltage is unstable and keeps a under voltage condition for T1 or a over voltage condition for T2, the FPOB/PGO states will be changed.

a) The anti-noise capacitor between VS12 and IS12 can suppress input noises and make more accurate OCP function.
b) Due to Class-3 ESD performance, the VS12 series resistance can be ignored and indirectly reduce OCP function error.

Pin-FPOB/PGO:

The FPOB and PGO are both open-drain devices. If AC turns on and PSU outputs are normal, VPGI > 1.2V and delay T8 continually, PGO state will keep at high through a resistance pulled to 12V output. Due to Class-3 ESD performance, the PGO series resistance can be ignored.
The FPOB is used to control the primary side PWM via an photo-coupler. A series resistance pulled to standby power is used to limit the opto-coupler and FPOB operation current. When IC is not ready or one of protect function is triggered, PSONB keeps at high state, the level of FPOB is high and the PWM will shut down.

Function & Application Descriptions (Cont.)

How to set output current protection:

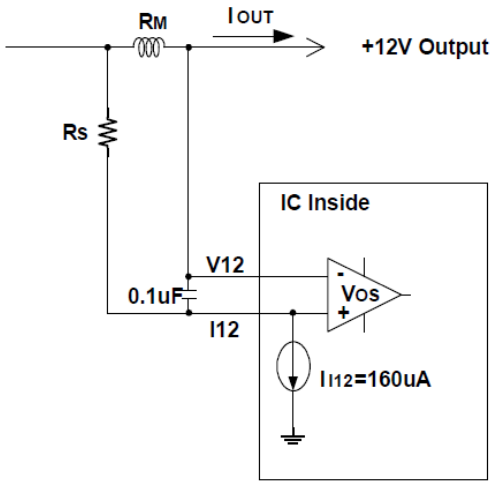
The parameters are IS12 pin sink current (II12), IS12 pin series resistance (RS), Output resistance (RM) and OP offset voltage (VOS). For example, we want to set 12VA output current “IOUT”

$$I_{OUT} \times R_M = I_{I12} \times R_S + V_{OS}$$

$$\Rightarrow I_{OUT} = \frac{I_{I12} \times R_S + V_{OS}}{R_M}$$

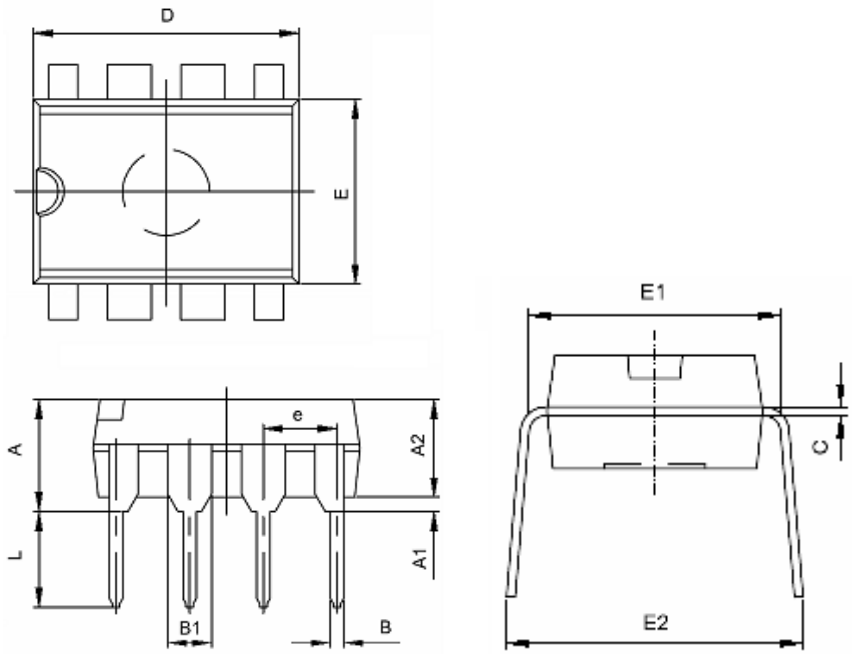
If I_{I12}=160uA, V_{OS} =0mV, R_S=250Ω, R_M=2mΩ

$$\Rightarrow I_{OUT} = \frac{160u \times 250 + 0m}{2m} = 20A$$



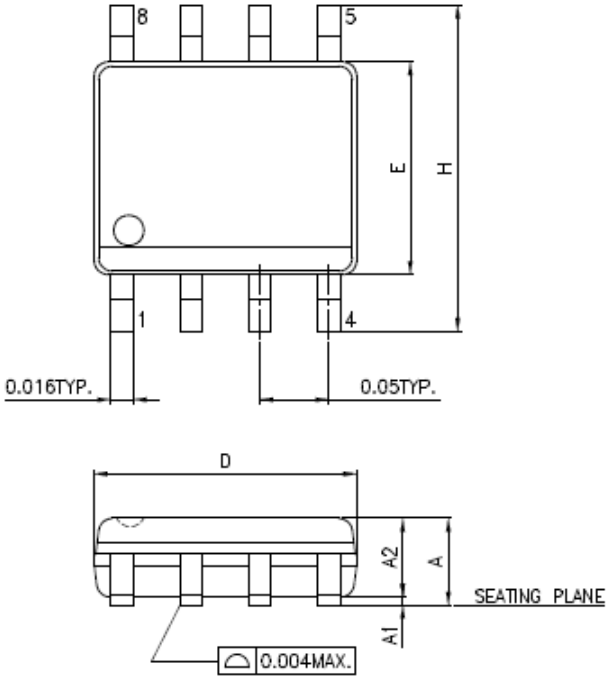
PACKAGING INFORMATION

DIP-8 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

SOP-8 Package （mm）

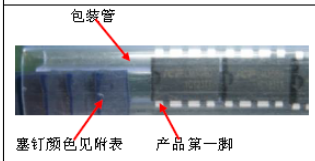
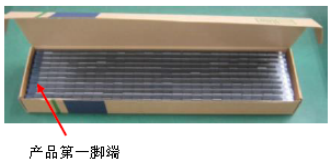
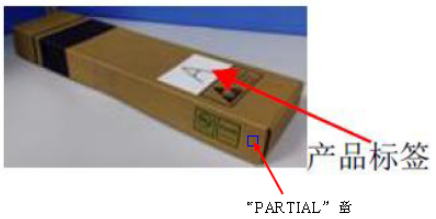


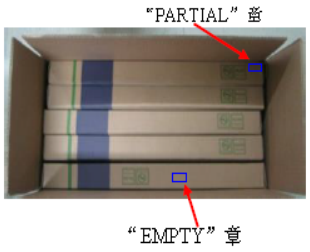
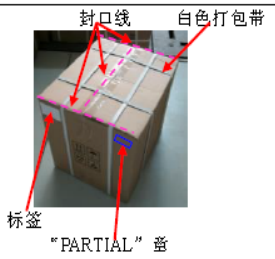
Symbols	Dimensions In Inches			Dimensions In millimeters		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	0.050	0.061	0.072	1.270	1.549	1.829
A1	0.000	------	0.010	0.000	------	0.254
A2	------	------	0.062	------	------	1.575
D	0.185	0.193	0.200	4.699	4.902	5.080
E	0.147	0.154	0.160	3.734	3.912	4.064
H	0.225	0.237	0.249	5.715	6.020	6.325
L	0.013	0.033	0.053	0.330	0.838	1.346
θ	0°	4°	8°	0°	4°	8°

Shipping Packing

DIP-8 / Tube data

材料	名称	包装管	通用管装气泡袋	通用管装包装盒	通用管装（1*10）包装箱
	规格	见附表	180*135（mm）	545*127*55（mm）	565*305*275(mm)
	图号	见附表	PTCN1380HTTY	PTCHG1255HTTY	PTCBG5630HTTY
	材质特点	PVC，无色透明	PVC，红色	三层单瓦楞	五层双瓦楞
	图片				

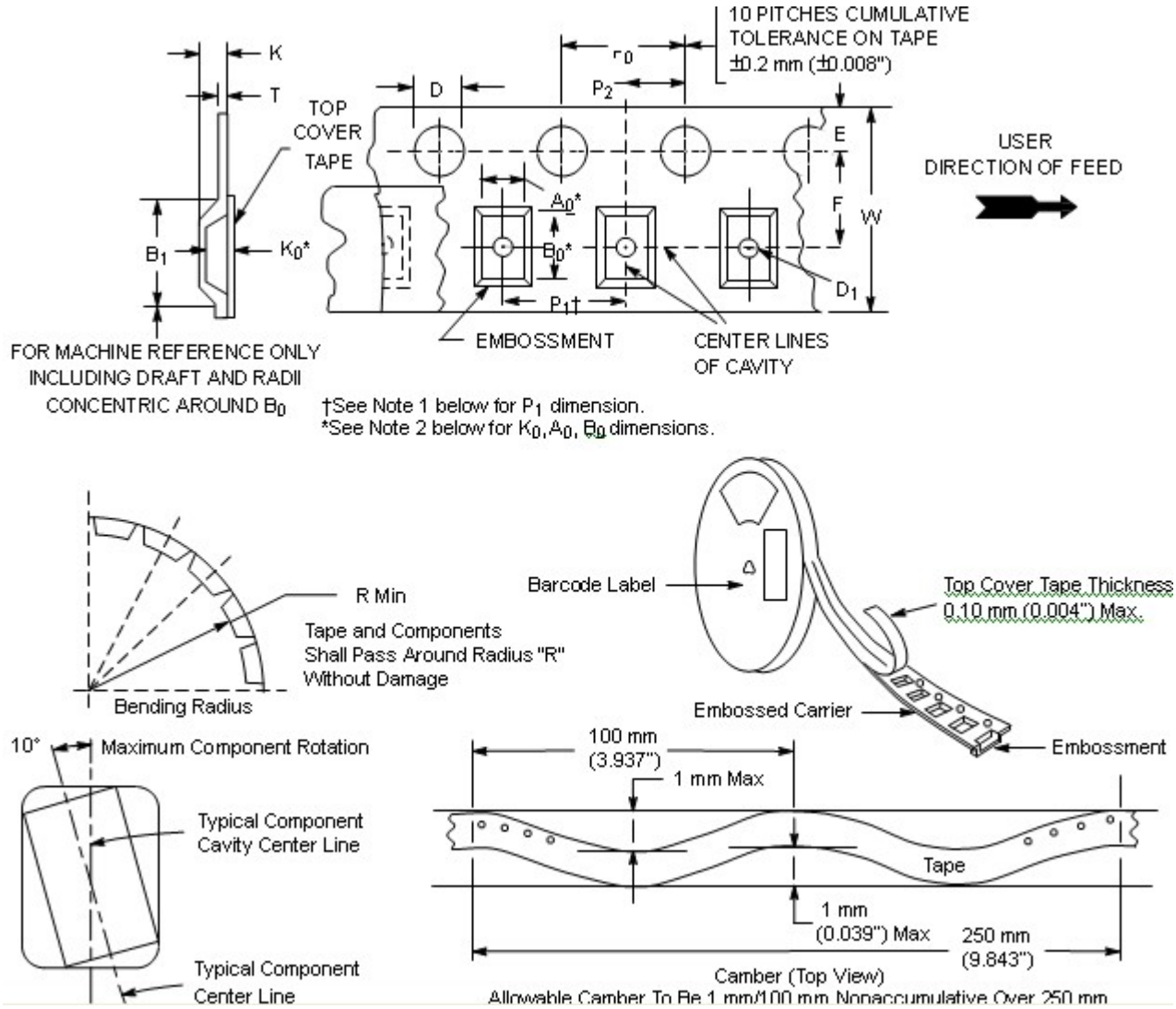
包装流程	产品在包装管中方向	放入包装盒	包装盒封口，贴标签
			
	1.产品第一脚朝向塞钉的颜色见附表（背面），包装管另一端为白色端。 2.所有产品在包装管中的方向一致。	1.将产品按图示方向放入包装盒。 2.每个工单批只能有一个不满管。不满管放在包装盒的最上层，方向与满管方向相反。	1.合住包装盒盖子，用宽胶带封口在包装盒图示位置贴产品标签。 2.是不满盒时，在包装盒上图示位置盖“PARTIAL”章。

装入包装箱，贴标签	包装箱封口，打包
	
1.如图示装入包装箱。 2.不满包装箱用空盒填满。空盒不贴任何标签，在图示位置盖“EMPTY”章。	1.包装箱上下面分别用宽透明胶带以“工”字形封口（即所有开口处都封住）。 2.如图贴产品标签，不满箱图示位置盖“PARTIAL”章。 3.用白色打包带以“井”字形打包，间隔匀称，垂直相交。

序号	包装数量					材料					
	封装形式	只/管	管/盒	盒/箱	只/箱	包装管图号	塞子颜色	销钉颜色	产品在包装管中第一脚塞子或销钉颜色	销钉位置	
1	DIP7L	50	40	10	20000	PTCGD0300HTTY04	蓝色	白色	蓝色塞子	第2孔	
2	DIP8L	50	40	10	20000	PTCGD0300HTTY04	蓝色	白色	蓝色塞子	第2孔	
3	DIP14L	25	40	10	10000	PTCGD0300HTTY04	蓝色	白色	蓝色塞子	第1孔	装有产品的包装管在包装盒中整齐放置

Embossed Tape and Reel Data Carrier Tape Specifications

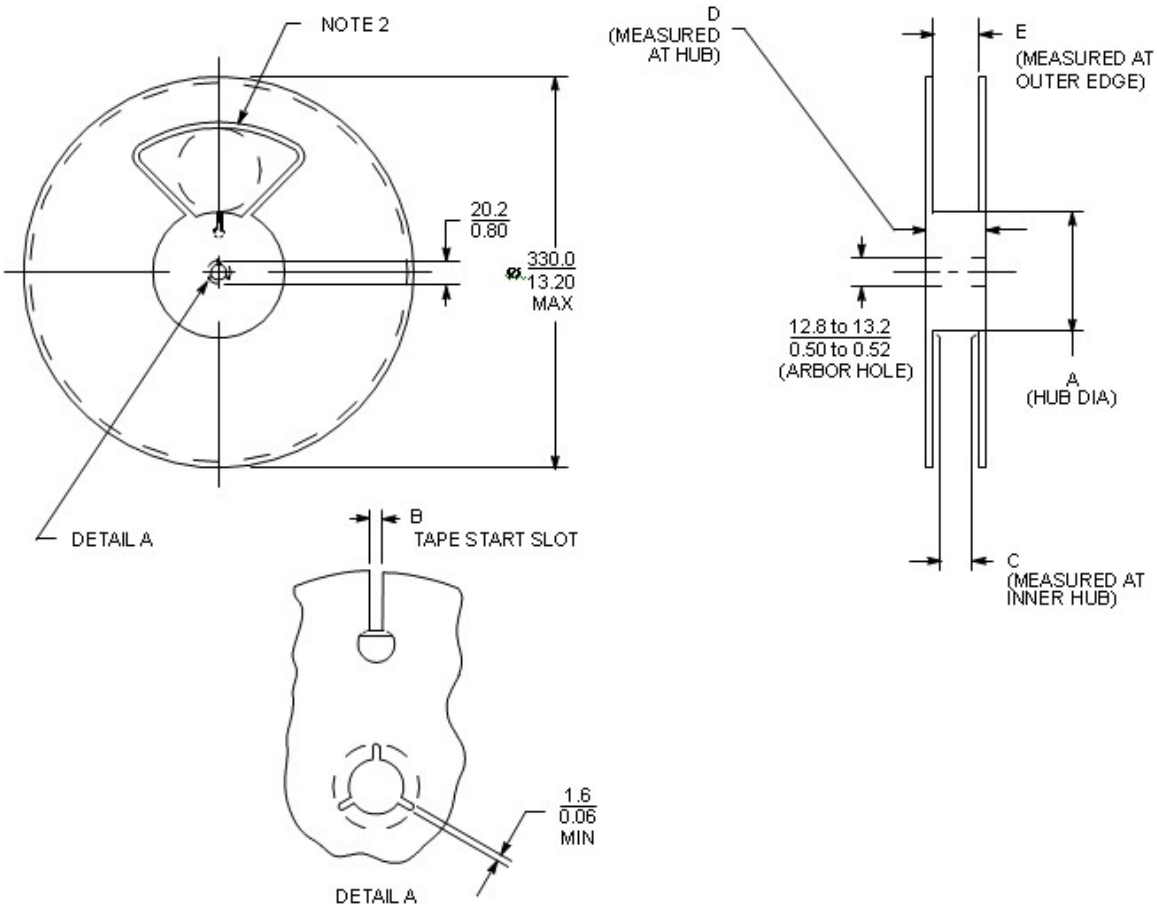
SOP-8/ Tape Reel Data



DIMENSIONS

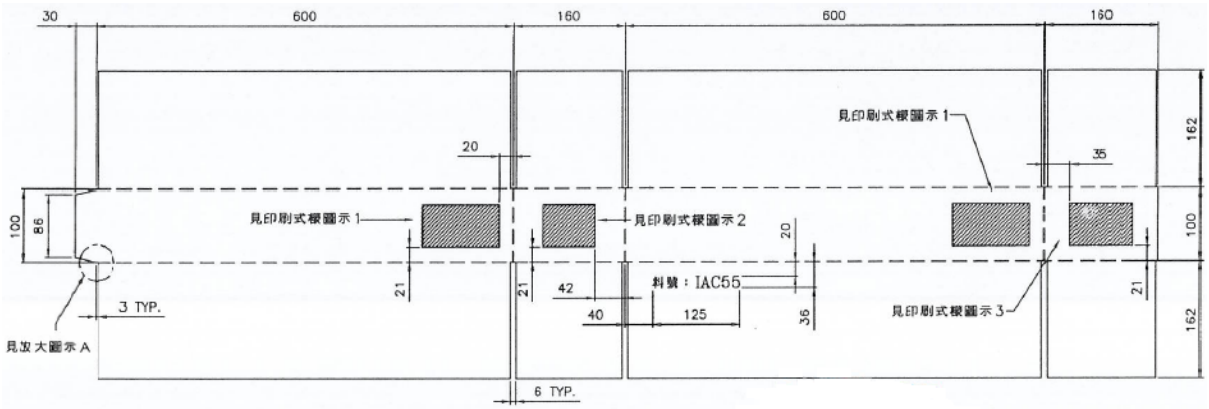
Tape ize (W)	B1 Max (Note 1)	D	D1	E	F	K	P0	P2	R Min	T Max	W Max
8 mm	4.55 mm (0.179")	1.5 + 0.1 − 0.0 (0.059 + 0.004" − 0.0)	1.0 Min (0.039") or 0.5 mm Min (0.020")	1.75 ± 0.1 (0.069 ± 0.004")	3.5 ± 0.05 (0.138 ± 0.002")	2.4 mm Max (0.094")	4.0 ± 0.1 mm (0.157 ± 0.004")	2.0 ± 0.1 mm (0.079 ± 0.002")	25 mm (0.98")	0.6 mm (0.024")	8.3 mm (0.327")
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060")		5.5 ± 0.05 (0.217 ± 0.002")	6.4 mm Max (0.252")			30 mm (1.18")		12 ± 0.30 (0.470 ± 0.012")
16 mm	12.1 mm (0.476")				7.5 ± 0.10 (0.295 ± 0.004")	7.9 mm Max (0.311")					16.3 mm (0.642")
24 mm	20.1 mm (0.791)				11.5 ± 0.1 (0.453 ± 0.004")	11.9 mm Max (0.468")					24.3 mm (0.957")

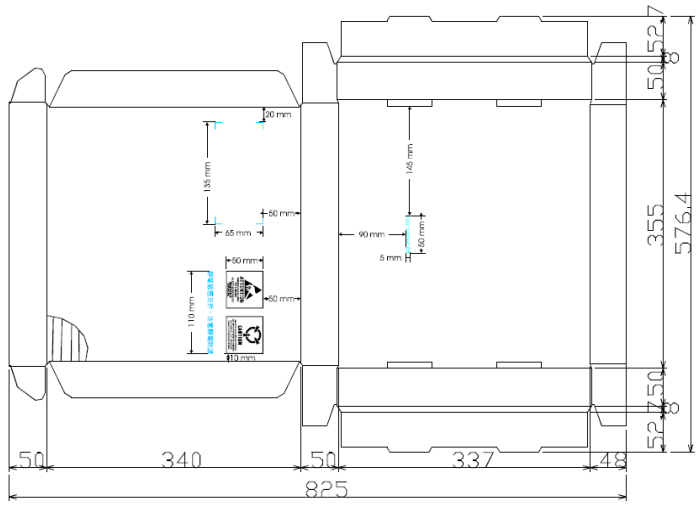
Reel Dimensions



Reel Diameter	Tape Size	A mm (inches)		B mm (inches)		C mm (inches)		D (Max)	E (Max)
		Min	Max	Min	Max	Min	Max		
178.0 (7.01)	16.0 (0.63)		50.0 (1.97)	6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)	178.0 (7.01)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	56.0 2.20	150.0 (5.91)		10.0 (0.39)	11.0 (0.43)	56.4 (2.22)	58.4 (2.30)	62.4 (2.46)	59.4 (2.34)
330.0 (12.99)	44.0 (1.73)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	44.4 (1.75)	46.4 (1.83)	62.4 (2.46)	47.4 (1.87)
330.0 (12.99)	32.0 (1.26)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	32.4 (1.28)	34.4 (1.35)	38.4 (1.51)	35.4 (1.39)
330.0 (12.99)	24.0 (0.94)	60.0 (2.36)		9.5 (0.37)	10.5 (0.41)	24.4 (0.96)	26.4 (1.04)	30.4 (1.51)	27.4 (1.08)
330.0 (12.99)	16.0 (0.63)			6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)			4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.01)	12.0 (0.47)	50.0 (1.97)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.47)	10.9 (0.43)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)

Tube Inner box Data

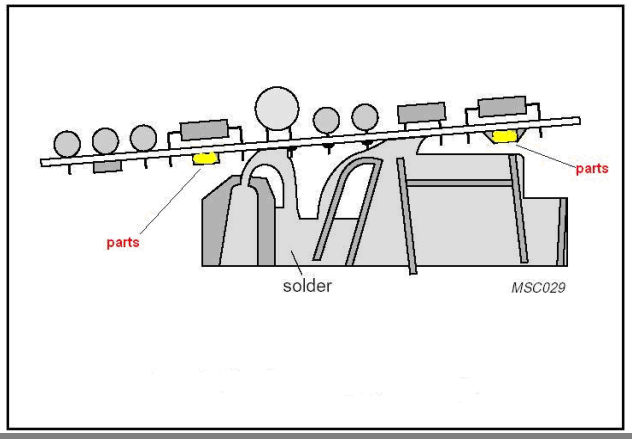
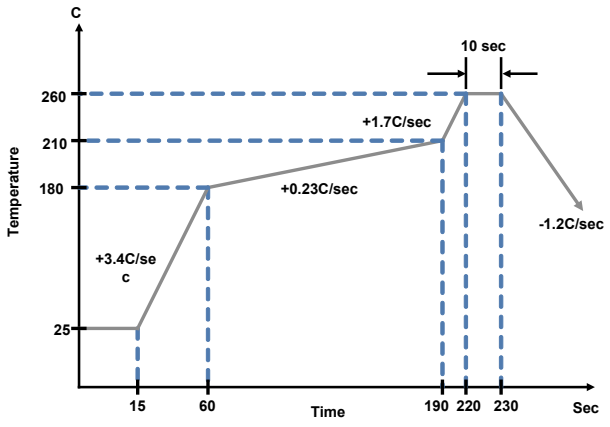




Reliability Test Program

SOP-8/DIP-8

Reflow Condition (IR/Convection or VPR Reflow)

Wave Soldering Process	IR Re-flow Soldering Curve
	

Test Item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245℃, 5sec
HOLT	MIL-STD-883D-1005.7	1000Hrs Bias@125℃
PCT	JESD-22-B,A102	168Hrs, 100% RH, 121℃
TST	MIL-STD-883D-1011.9	-65℃~150℃, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHMB>2KV, VMM>200V
Latch-Up	JESD 78	10ms, 1tr> 100mA

Revision History

REVISION	DESCRIPTION	PAGE	DATE
Rev 1.0	First release	13	2007/06/18