Data Sheet

Type Description : Green-Mode PWM Controller

Product Name : EST.3200xS

Reversion : V1.1

Reversion Date : 10, 2021

Page : 16 Pages

General Description

The EST.3200xS is a higher integrated multi-mode flyback controller suitable for designing high-performance off-line power converters. It provides several functions to enhance the efficiency to meet the criteria of global standards such as DoE Level VI and EU CoC V5 Tier-2.

Meantime, it also provides excellent EMI-improved solution, and also builts in all complete protection.

To increase various load performance, the EST.3200xS family features a green mode function, which implements low start-up current, green-mode power-saving. It is also built-in the leading-edge blanking (LEB) of the current sensing and feedback loop to screen the spike noise from any input signal. The internal slope compensation can limit the constant output over universal AC input range. The sawtooth over frequency function for EMI improved solution.

Meanwhile, to ensure system ruggedness , the EST.3200xS is also implements various protection, such as, OLP (Over Load Protection) ,VDD OVP (Over Voltage Protection) , Output OLP and output OVP to prevent the circuit damage from the abnormal conditions.

Application

- Switching AC/DC adapter and battery charger
- ATX standby power
- Open frame switching power and CD(R) Set-top-boxes(STB) 384Xreplacement

Features

- Integrated 700V Start-Up Device
- Brown-In and Brown-Out
- EST.3200DS=65KHz/3200MS=100KHz/3200HS= 135KHz fix frequency mode at PWM Mode
- 0.5mA ultra-low operating current at light load
- Current mode control with Cycle-by-Cycle current limit
- Built-in slope and load regulation compensation
- LEB (Leading-edge blanking) on CS Pin
- UVLO (Under voltage lockout)
- Fault Protections : VDD Over Voltage, CS OVP(Over Voltage), Output Short-Circuit, Over-Current, OLP (Over load protection) , External Over Temperature (OTP) and Pin Fault
- Photo coupler short & Feedback open protection
- High voltage CMOS process with excellent ESD protection
- 250mA/-500mA driving capability
- Hazardous Substance Free
- RoHs/REACH Compliant

SOP-8L

***EST.3200xS works with current sensing synchronous rectifier controllers, such as EST.6001C/6002A, to achieve higher conversion efficiency and very compact power density.

Function and Protection Options

Part No.	Package	Freq. KHZ	Protection						
			OLP	VDD OVP	CS OVP	OTP	CS Open	SDSP	BNO
EST.3200DS	SOP-8	65KHz	Hiccup / 100ms	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup
EST.3200MS	SOP-8	100KHz	Hiccup / 65ms	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup
EST.3200HS	SOP-8	135KHz	Hiccup / 48ms	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup

Ordering Information

Part Number	Package	Packaging	Note
EST.3200DS & ASR	SOP-8L	Tape & Reel	Green
EST.3200MS & RSR	SOP-8L	Tape & Reel	Green
EST.3200HS & LSR	SOP-8L	Tape & Reel	Green

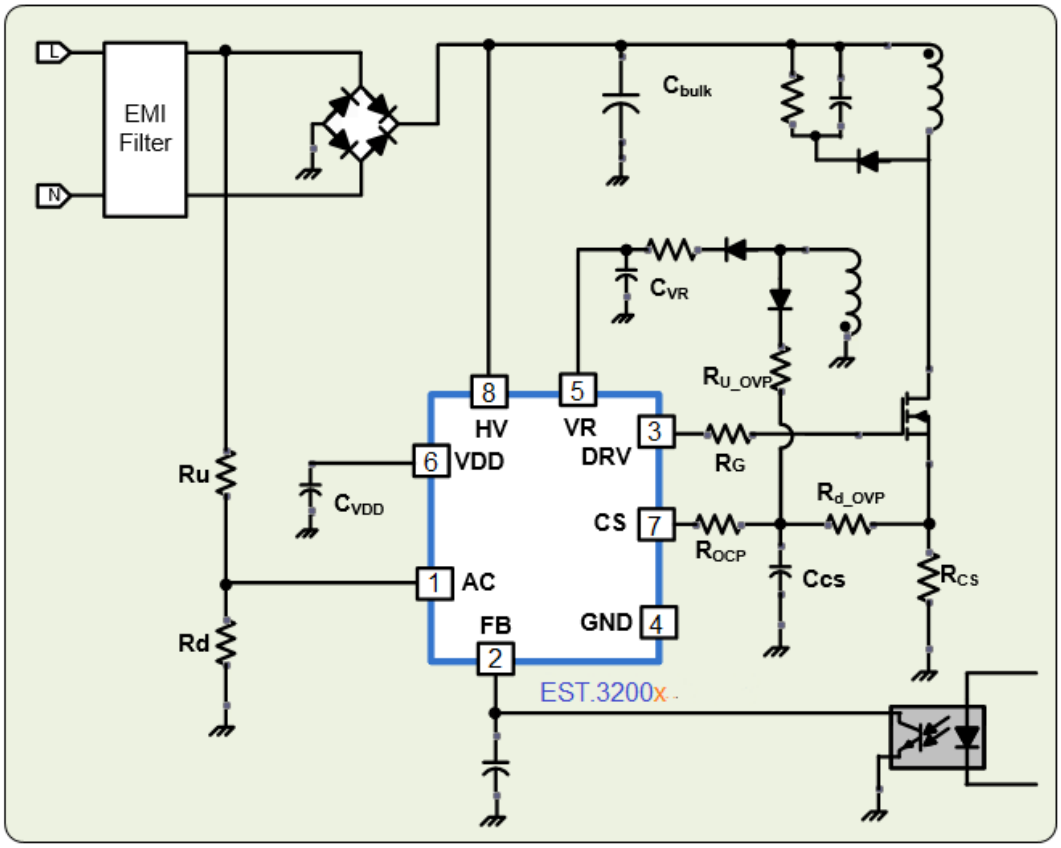
Note: EST lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. EST lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. EST defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

Pin Assignments and Package Type

EST: LOGO
3200xS:
3200= Part Number
xS = Frequency Type
XXXX: Production lot code
Y: Year code
WW : Week code

SOP-8L	NAME Description	Description
1	AC	AC/DC Brown in/out (option, can floating)
2	FB	Voltage input pin by connecting a photo-coupler
3	DRV	Driver output to driver the external MOSFET
4	GND	Ground
5	VR	Connect auxiliary winding to provide IC power supply
6	VDD	Power supply pin
7	CS	Current Sense input. The current sense resistor between this pin and GND is used for current limit setting.
8	HV	High Voltage Input for Start-Up. This pin can withstand high voltage up to 700V.

Application Circuit



Absolute Maximum Ratings

Parameter Symbol		Symbol	Limit Values		Unit	Remark
			Min.	Max		
Supply Voltage VDD		V_{DD}	-0.3	32	V	
FB,CS,RTL		V_{FB} V_{CS} V_{RTL}	-0.3	7	V	
HV to GND		V_{HV}	-0.3	700	V	
VR to GND		V_{VR}	-0.3	120	V	
Gate Driver Voltage		V_{DRV}	-0.3	V_{DD}+0.3	V	
Gate Output Current		I_{DRV}		500	mA	
Max Junction Temperature		T_{jm}	-40	150	℃	
Operation Junction Temperature		Tj	-40	125	℃	
Operation Ambient Temperature		T_A	-25	85	℃	
Storage Temperature		T_{stg}	-55	150	℃	
Absolute Max. IDD Current @ V_{DD}=25V	Ta = 25℃	I_{DD_max}	-	22	mA	SOP-8
Power Dissipation @TA=85℃		P_D	-	556	mW	
Junction-to-Ambient Thermal Resistance*		θ_{JA}		180	℃/W	
Junction-to-Case Thermal Resistance**		θ_{JC}		39	℃/W	
Lead temperature (Soldering, 10 sec)			-	260	℃	
ESD Voltage Protection	HBM	$V_{ESD-HBM}$	-	3.0	KV	
	MM	V_{ESD-MM}	-	300	V	

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
Supply Voltage VR	V_R	12	100	V	
Capacitance of CS pin	C_{CS}	47	680	pF	D_{CS}
CS Diode (D_{CS})	trr		150	ns	1N4148
CS OVP	R_{d_OVP}	100	400	Ω	
Ambient temperature range	Topr	-40	85	℃	
Capacitance of FB pin	C_{FB}		2.2	nF	

DC Electrical Characteristics (VCC =15V, Ta=25°C)

HV Section (VHV Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
IHV Supply Current for HV pin	I_{HV-ST1}		4		mA	VDD < UVLO ON, V_{HV}=200V
Off State Leakage Current	I_{HV-LK}		1		μA	VDD > UVLO ON, V_{HV}=560V

Supply Voltage (VDD Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Current (with 1nF load on DRV pin)	I_{CC-OP}	0.3	0.6	0.8	mA	V_{FB}=0V
	I_{CC-OP}	1	2	2.3	mA	V_{FB}=2.5V CL=1nF
	I_{CC-OLP}	0.45	0.55	0.65	mA	Protection Current
UVLO (off)	$V_{UVLO-OFF}$	7.5	8.0	8.5	V	
UVLO (on)	$V_{UVLO-ON}$	16	18	19	V	
VDD OVP Level	V_{OVP}	26	27	28.5	V	
OVP Debounce Time	T_{OVP}		4		cycle	Guarantee by Design
VDD Simulation mode(ON)	VDD_{-HD_ON}	9.5	10.2	10.5	V	
VDD Simulation mode Hysteresis Voltage	VDD_{-HD_HYS}	0.5	1	1.5	V	

High Voltage Regulation (VR Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage	V_{VR}	12		100	V	
Regulation Voltage	V_{VDD}	17	18	19	V	V_{VR}=21V , I_{VDD} <=20mA

Voltage Feedback(FB Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	J_{Zero}	0.1	0.14	0.18	mA	V_{FB}=0V
Open Loop Voltage	V_{FB-OP}	4.8	5	5.2	V	FB pin open
Over Load Protection	V_{OLP}	3.5	4	4.5	V	
Debounce Time of OLP	T_{OLP}	90	100	110	ms	EST.3200DS
		55	65	75	ms	EST.3200MS
		38	48	58	ms	EST.3200HS
Burst mode start voltage(on)	V_{BUR_ON}	--	0.45	--	V	
Green Mode Threshold	F_{th_GR}	35	45	55	KHz	V_{FB}=1.3V EST.3200DS
		50	60	70	KHz	V_{FB}=1.3V EST.3200MS
		70	80	90	KHz	V_{FB}=1.3V EST.3200HS

Current Sensing (CS Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time & Propagation Delay to Output	T_{LEB} +T_{PD}	400	500	600	ns	
Maximum CS Off Voltage	V_{CSTH}	0.66	0.7	0.74	V	
OCP source current	I_{OCP}	240	250	260	uA	Min. Duty
CS Over Voltage Protection	V_{CS_OVP}	0.45	0.5	0.55	V	T = T_{off}
CS OVP De-bounce Time	T_{CS_OVP1}		4		cycle	V_{CS}> V_{CS_OVP} & V_{FB}> V_{OLP}
	T_{CS_OVP2}	90	100	110	ms	EST.3200DS
		55	65	75		EST.3200MS
		38	48	58		EST.3200HS
OVP Leading Blanking time	T_{OVP_LEB}		2		us	Guarantee by Design
Internal Slope Compensation*	$V_{SLP\_LP\_LEB}$		160		mV	
Short Circuit Protection Voltage	V_{SCP}		0.85		V	
Debounce Time of VSCP	T_{SCP}		2		cycle	
Short Circuit Detection Time	T_{SCP}		100		us	

Alternating Current Detect (AC Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Brown In trigger point	V_{BNI}	0.65	0.7	0.75	V	
Brown Out trigger point	V_{BNO}	0.55	0.6	0.65	V	
BNO De-bounce time	T_{BNO}	20		25	ms	EST.3200D
		13		19,5		EST.3200M
		9.5		10.6		EST.3200H

Driver(DRV Pin) :

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output Low Level	V_{OL}			1	V	VDD = 16V, IO=20mA
Output High Level	V_{OH}	8			V	VDD = 16V, IO=20mA
Output Clamp Voltage Level	V_{G_Clamp}	11	12.5	14	V	VDD = 25V
Rising Time	T_R	200	300	400	nS	VDD = 16V, CL= 1nF
Falling Time	T_F	10	30	50	nS	VDD = 16V, CL= 1nF

Timer Section:

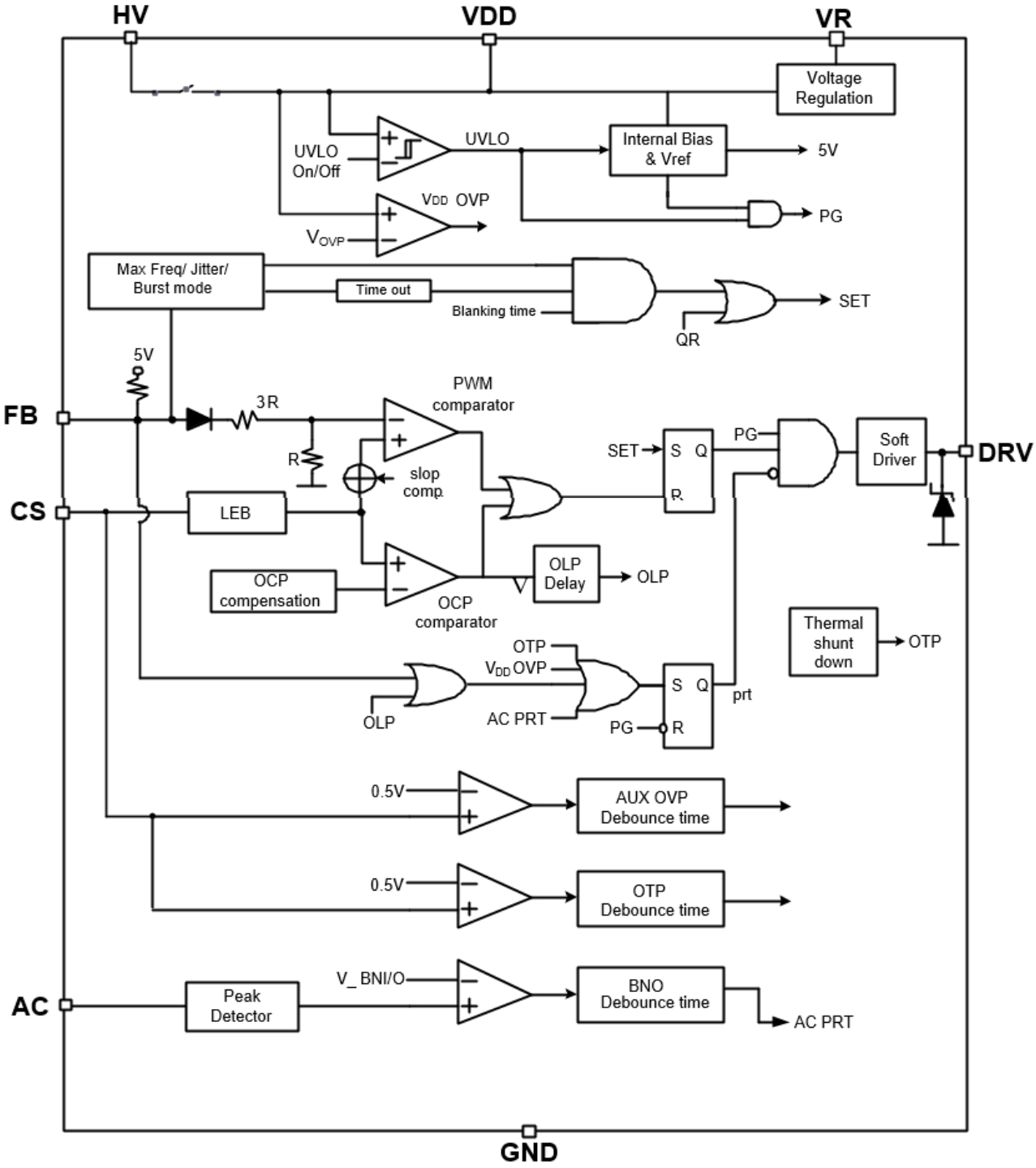
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F_{Burst}	22		28	KHz	
PWM Mode Frequency	F_{PWM}	61	65	69	KHz	EST.3200DS
		95	100	105		EST.3200MS
		130	135	140		EST.3200HS
Voltage stability of Frequency	F_{PSRR}	-1		+1	%	VDD = 11V~25V
Frequency Shuffling Range	F_{jitter}	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D_{MAX}	75	80	85	%	
Internal Soft Startup Time	T_{SS}	10.3	13.2	16.2	mS	EST.3200DS
		6.7	8.6	10.5		EST.3200MS
		4.9	6.4	7.8		EST.3200HS

On chip OTP:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
OTP Level			150		℃	
OTP exit			120		℃	

Block Diagram

EST.3200xS



Application Note

Operation Overview

The EST.3200XS family meet the green power requirement and very is suitable for the application for those networking adaptors, TV open frame and various consumer power, which can provide more power efficiency and lower power loss. It also supports various kind of protection for every abnormal environments.

SS，Soft-start Sequence

EST.3200XS also built-up T_{SS} soft-start to soften the electrical stress occurring in the power supply during startup, refer to fig.1. As soon as VDD reaches UVLO_on, the Cs peak voltage is gradually increased from 0.2V to the maximum level, see fig.1.

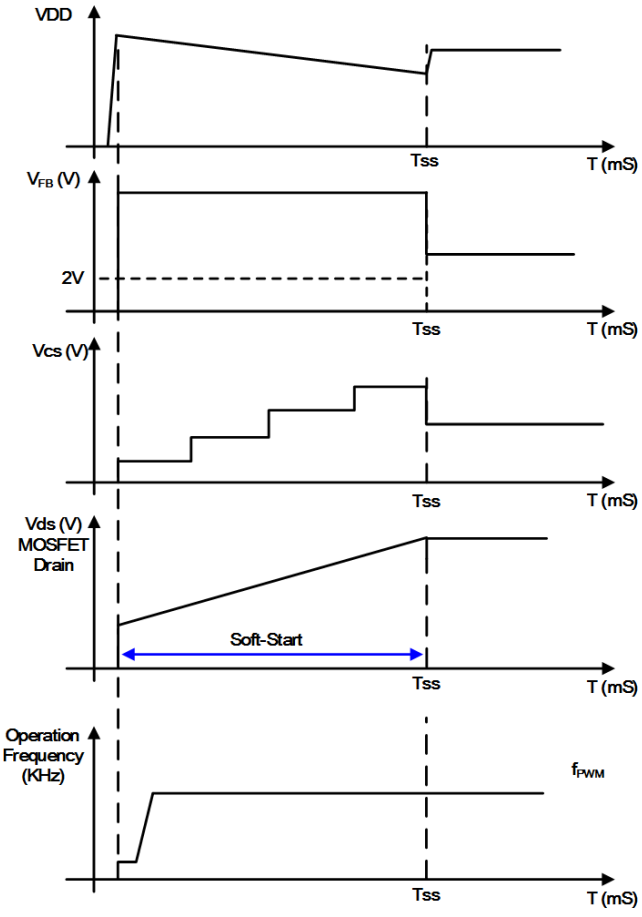


Fig.1

FB，Voltage Feedback Loop

EST.3200XS series adopt current mode control, that is say, the voltage feedback signal is provided from TL431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

(1). R_{bias1} and R_{bias2} to prevent the abnormal output voltage at heavy loading. Generally, we suggest R_{bias1} 100~1KΩ，R_{bias2} 1.5~2.5KΩ

(2). R_{phase}/C_{phase} is for RC phase compensation and prevent oscillate to adjust the value of C_{FB}

(3). Generally, we suggest R_{phase} 1~10KΩ，C_{phase} 0.1uF ，CFB 1~2.2nF

(3). The ratio of R_3 and R_{3A} is depent on the output voltage spec (TL431 ,V= 2.5V)

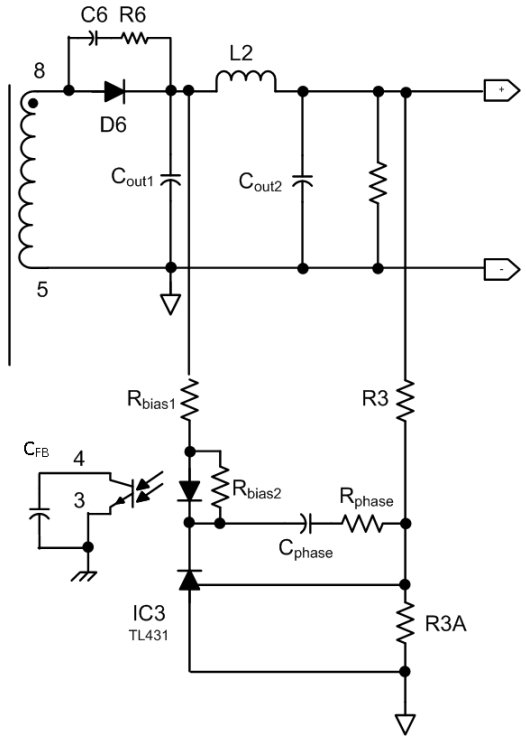


Fig.5

In addition, V_{FB} is also used to determine the green mode level .When V_{FB} is under V_{BUR_ON} , it is under no load or light load condition; at light loading, burst mode can effectively reduces the switching loss.

When V_{FB} is larger than V_{BUR_ON}, it will leave away the standby mode. The normal operation of V_{FB} is from V_{BUR_ON} to 2.4V,; meanwhile, short-circuit current is around I_{Zero}

CS, Current sense Loop

Current mode PWM control mode detects the current command (CS) from the Rsense (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continues conduction mode (CCM) , therefore, EST.3200DS/MS/HS series of built-in high and low slope compensation to avoid the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS pin being damaged by the unknow negative spike.

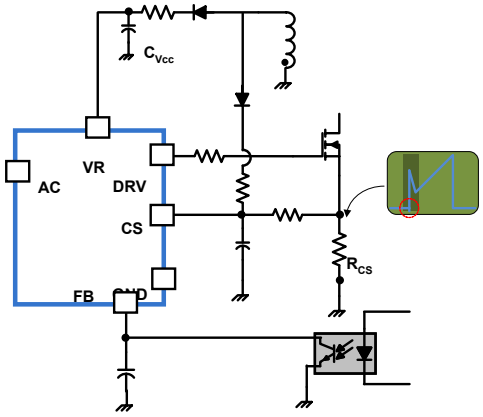


Fig.6

DRV

The driving capability of EST.3200XS is around 450mA, which can support power rate around 60~70W, and it is limited the maximum duty-cycle below 80% to avoid the
transformer saturation.

Typically, the threshold of MOSFET is about 20V, and the maximum clamp voltage of EST.3200XS is 14V to prevent breakdown of MOSFET.

Complete Protection

EST.3200XS integrates various kind of protection to make sure operation safety.

SDSP, Secondary Diode Short Protection

After short circuit of 2nd side schottky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high Vds to damage MOSFET.

EST.3200XS detects the inductance current through the resistance, Rcs, of CS pin, and will trigger protection (latch or hiccup) when Vcs higher than 0.85V and sustains 2cycle timing.

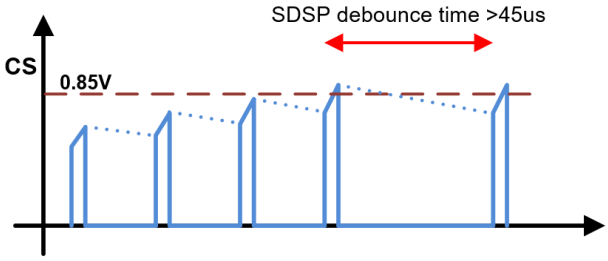


Fig.8

AC, Brown-in/out

EST.3200XS provides real detection of AC line through AC pin connected directly to AC line. When the VDD of EST.3200XS reaches UVLO_ON , it is into the state of AC detection ,and sustains a delay time T_{ADC} .This AC pin is used to program the AV over and under voltage level through a resistive divider (Ru/Rd).

If Vac is lower than below V_{BNI}, it will turn-off the output till next cycle to check the condition is removed or not. Even after it turn-off, this pin is continues to detect line status. If Vac is lower than below V_{BNO} for the timing T_{BNO} , it will be turn-off , and re-start again.

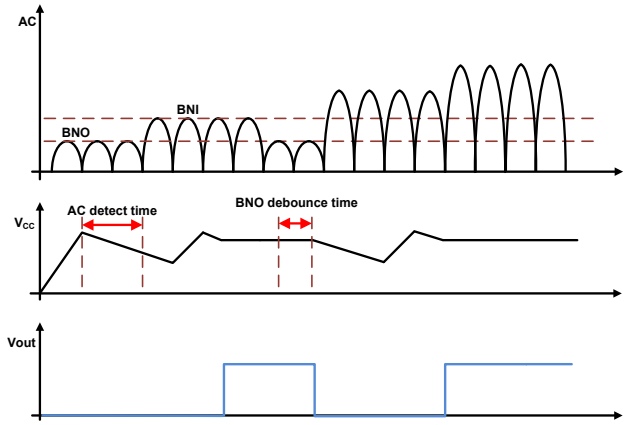


Fig.9

Layout Guide line

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

- ✓ **Big current path** : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area
- ✓ **Low voltage area :** R devider need to be as near FB_Pin as possible.
- ✓ **Secondary Side Schottky :** routing as close as possible
- ✓ **Grounding :** (2).(3) and (4) grounding separated with each other, and end connects to (1) ground.

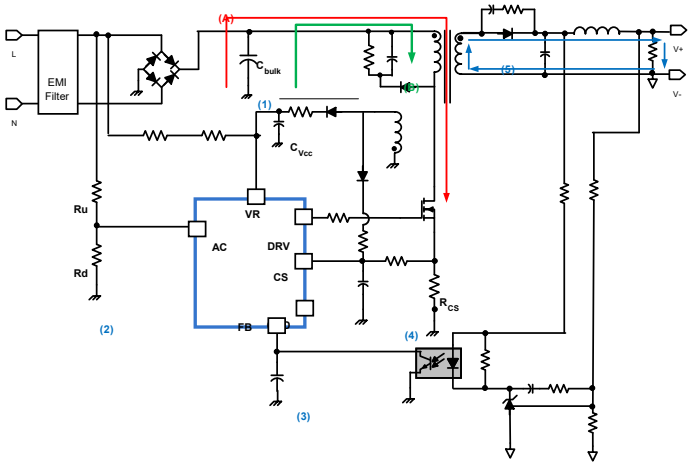


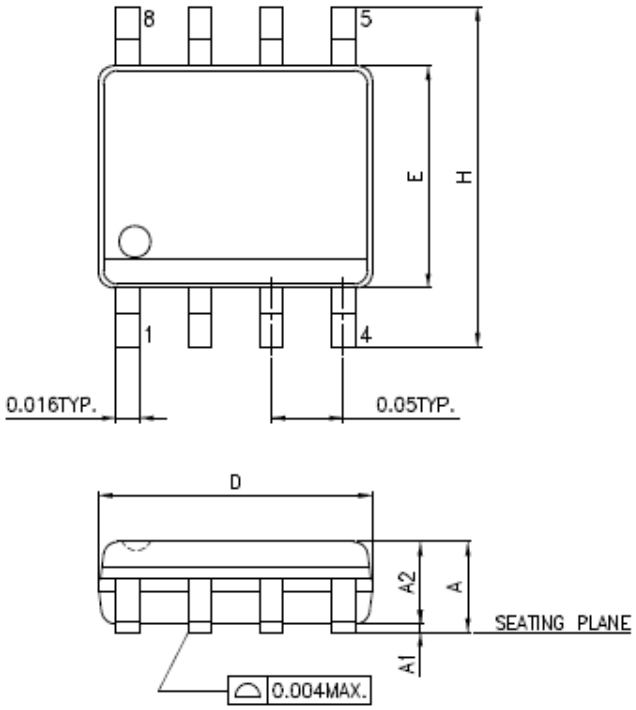
Fig.10

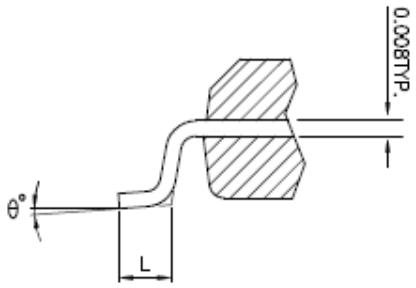
Table 1: Complete Protection

Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VDD UVLO Off	VDD	VDD < 7.5V
1st	AC pin	Brown In Fail	AC	V_{AC}<0.85
1st	AC pin	Brown out	AC	V_{AC}>0.7V
1st	V-Sense	CS pin open	CS	V_{CS} >0.7V after 4 cycles
2nd	SDSP	2nd side Schottky short	CS	VCS >0.85V after 2 cycles
2nd	SCP	Output short	CS	1. 12ms blank time during start-up 2. after 4 cycles 3.Duty < 10%
2nd	OVP	Output OVP	CS	Vcs compares to 0.5V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS=0.7V
2nd	OLP	OLP	FB	CS > 4V
IC	Chip OTP			chip OTP at 150 ℃

Package Information

SOP-8 Package (mm)

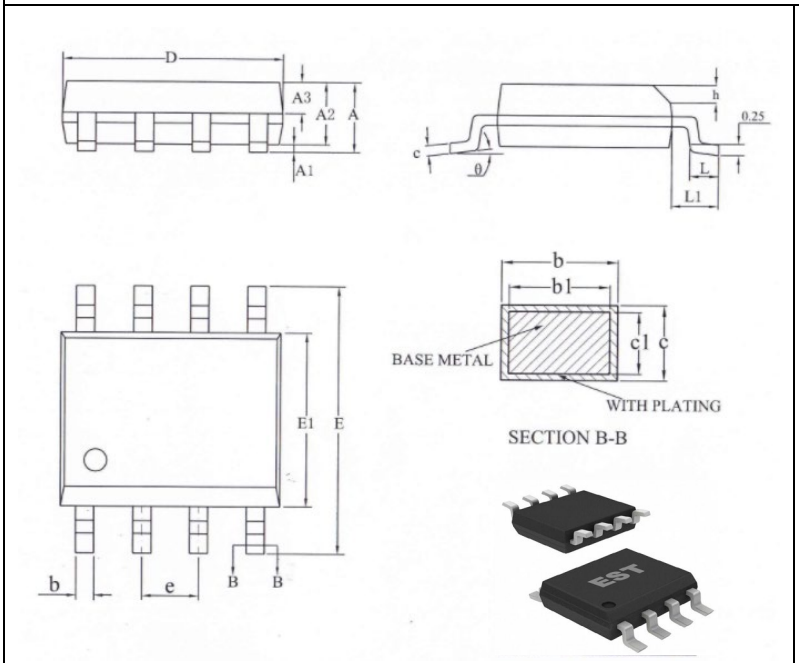




Symbols	Dimensions In Inches			Dimensions In millimeters		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	0.050	0.061	0.072	1.270	1.549	1.829
A1	0.000	------	0.010	0.000	------	0.254
A2	------	------	0.062	------	------	1.575
D	0.185	0.193	0.200	4.699	4.902	5.080
E	0.147	0.154	0.160	3.734	3.912	4.064
H	0.225	0.237	0.249	5.715	6.020	6.325
L	0.013	0.033	0.053	0.330	0.838	1.346
θ	0°	4°	8°	0°	4°	8°

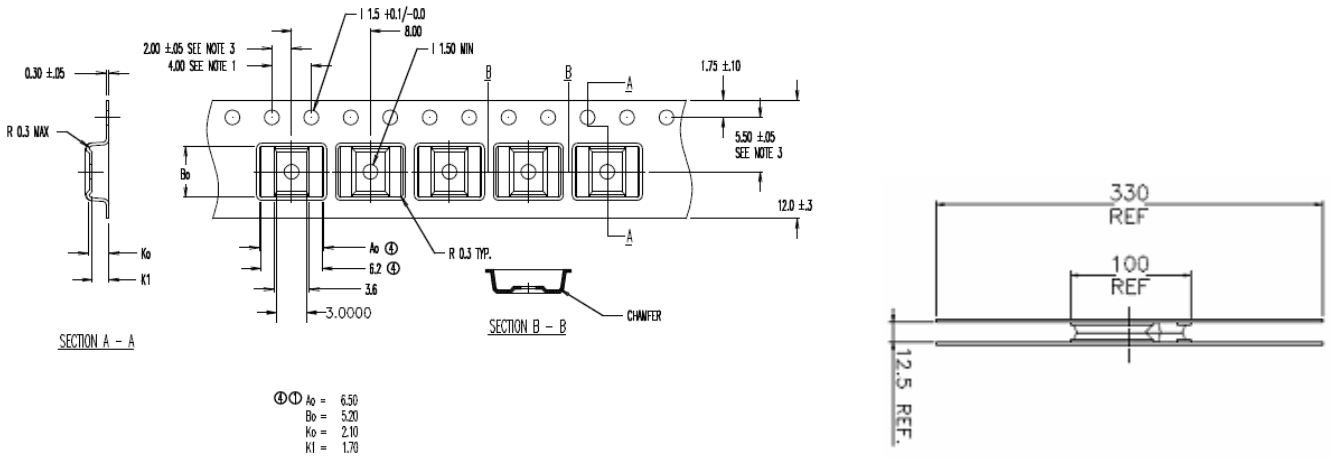
Package Information

SOP-8

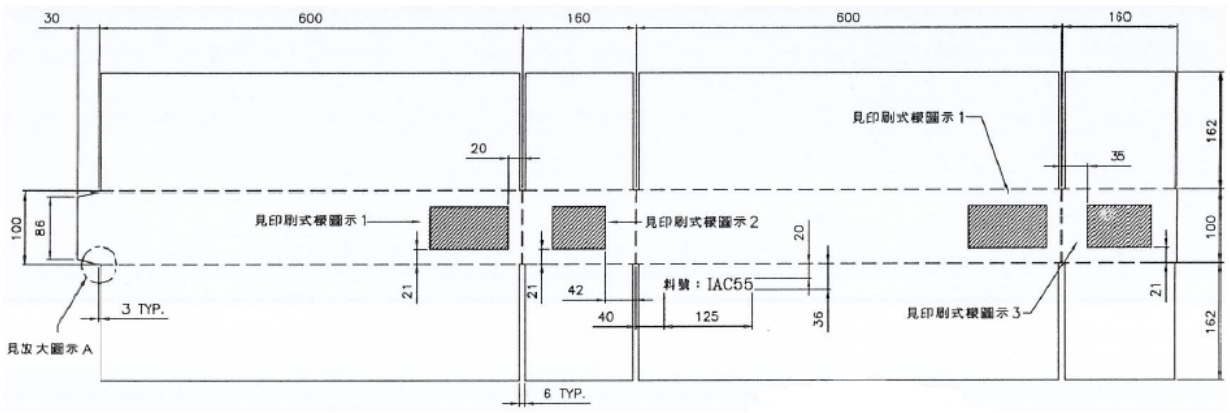


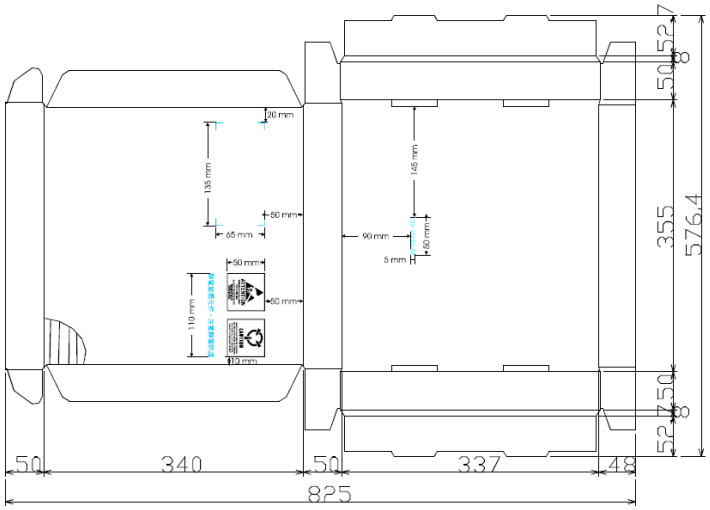
Symbol	Dimension in mm		
	MIN	NOM	MAX
A	--	--	1.75
A1	0.1		0.225
A2	1.3	1.4	1.5
A3	0.6	0.65	0.7
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.2	--	0.24
c1	0.19	0.2	0.21
D	4.8	4.9	5
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.27BSC		
h	0.25	--	0.5
L	0.5	--	0.8
L1	1.05REF		
θ°	0°	--	8°

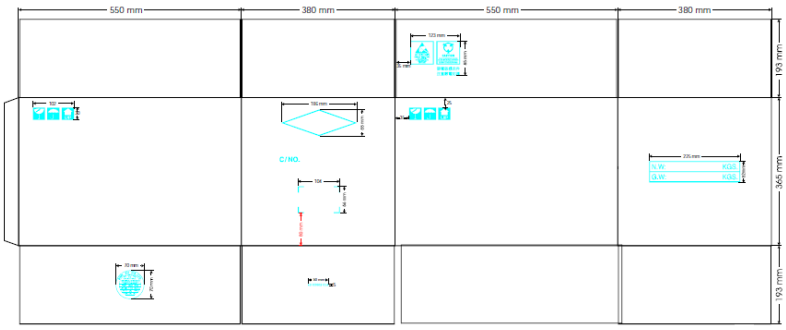
SOP-8 / Tape Reel Data



Tube Inner box Data







NOTE
1.紙箱尺寸：L550 X W380 X H365 mm
2.尺寸公差：± 5 mm
3.紙箱材質：面紙白紙 240
蕊紙 B 浪 100
中紙 175
蕊紙 A 浪 180
底紙 A 級 200
4.破裂強度：250LBS ± 10LBS
5.印刷顏色：天空藍
6.備 註：紙箱打釘

Revision History

REVISION	DESCRIPTION	PAGE	DATE
V1.0	First Release		2021/10/22
V1.1	Correction of errors	P3	2021/10/22