Data Sheet

Type Description : Green-Mode PWM Flyback (SSR) Controller

Product Name : EST.30xxMS

Reversion : V1.0

Reversion Date : May, 2021

Page : 17 Pages

General Description

EST.30xxMS is a higher integrated PWM flyback controller. It provides several functions to enhance the efficiency to meets the criteria of global standards such as DoE Level VI and EU CoC V5 Tier-2. Meantime, it also provides excellent EMI-improved solution, and also built in complete protection.

EST.30xxMS is a green mode controller, which implements low start-up current, green-mode power-saving. It is also built-in the leading-edge blanking (LEB) of the current sensing and feedback loop to screen the spike noise from any input signal. The internal slope compensation can limit the constant output over universal AC input range. The sawtooth over frequency function for EMI improved solution.

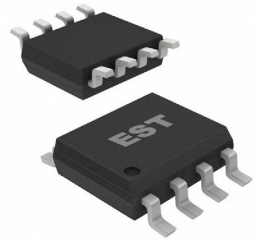
Meanwhile, EST.30xxMS also provides various protection, such as, OLP (Over Load Protection) ,VDD OVP (Over Voltage Protection) , Output OLP and output OVP to prevent the circuit damage from the abnormal conditions.

EST.30xxMS is available in SOP-8.

EST.30xxMS works with current sensing synchronous rectifier controllers, such as EST.6002A or EST.6xxAxxC to achieve higher conversion efficiency and very compact power density.

Features

- Integrated 650V/ 700V /800V/ Start-Up Device and MOSFET
- 100KHz fix frequency mode at PWM Mode
- Very low startup current (<3 uA)
- Soft Driving for Reducing EMI Noise
- 0.5mA ultra-low operating current at light load
- Current mode control with Cycle-by-Cycle current limit
- Built-in slope and load regulation compensation
- LEB (Leading-edge blanking) on CS Pin
- UVLO (Under voltage lockout)
- Fault Protections : VDD Over Voltage, Output Short-Circuit, Over-Current, OLP (Over load protection) and Pin Fault
- Photo coupler short protection & Feedback open protection
- High voltage CMOS process with excellent ESD protection
- 250mA/-500mA driving capability
- Hazardous Substance Free
- RoHs/REACH Compliant



SOP-8L

Application

- Switching AC/DC adapter and battery charger
- ATX standby power
- Open frame switching power and CD(R)
- Set-top-boxes(STB) 384Xreplacement

Function and Protection Options

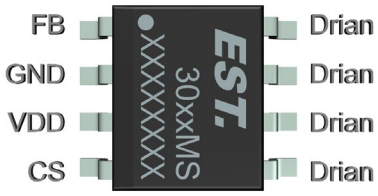
Part No.	Package	Freq.	Protection				
		KHZ	VCC OVP	OLP(65mS)	CS Open	SDSP	Line OVP
EST.30xxMS	SOP-8L	100KHz	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup

Note: EST lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. EST lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. EST defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

Ordering Information

Part Number	Package	Packaging	Note
EST.30xxMS	SOP-8L	Tape	Green

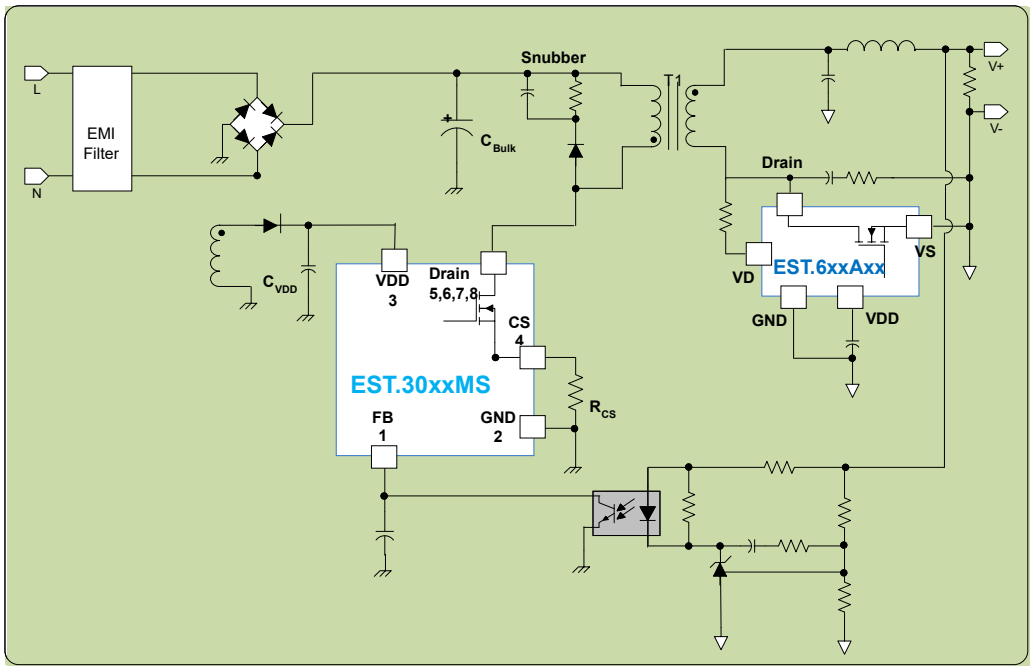
Pin Assignments and Package Type



EST: LOGO
30xxMS: xx=MOS Type;
M=100KHz
S= Smd
XXXXXXX: Production lot code

SOP-8	NAME Description	Description
1	FB	Voltage input pin by connecting a photo-coupler
2	GND	Ground
3	VDD	Power supply pin
4	CS	Current Sense pin, connect to sense the MOSFET current.
5,6,7,8	Drain	For start-up, the pin is also HV power MOSFET drain pin

Application Circuit



Absolute Maximum Ratings

Parameter Symbol		Symbol	Limit Values		Unit	Remark
			Min.	Max		
Supply Voltage VDD		V_{DD}	-0.3	32	V	
FB,CS Voltage		V_{AC},V_{FB},V_{CS},	-0.3	7	V	
Drain Voltage		V_D	660		V	
Max Junction Temperature		T_{jm}	-40	150	℃	
Operation Junction Temperature		Tj	-40	125	℃	
Operation Ambient Temperature		TA	-25	85	℃	
Storage Temperature		T_{stg}	-55	150	℃	
Absolute Max. IDD Current @ V_{DD}=25V	Ta = 25℃	I_{DD_max}	-	22	mA	SOP-8
Power Dissipation		PD	-	556	mW	
Junction-to-Ambient Thermal Resistance*		θ_{JA}	-	180	℃/W	
Junction-to-Case Thermal Resistance**		θ_{JC}	-	39	℃/W	
Lead temperature (Soldering, 10 sec)			-	260	℃	
ESD Voltage Protection	HBM	$V_{ESD-HBM}$	-	3.0	KV	
	MM	V_{ESD-MM}	-	300	V	

*1All items are tested with the standards JESD 51-2 and 51-10(DIP).
Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.
*2. Free standing with no heatsink; withoud copper clad (Measeurment condition: just before junction temperature Tj, enters into OTP)
*3.Measure on the DRAIN pin close to plastic interface

Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
Supply Voltage VDD	VDD	11	25	V	
Startup Resistor Value	R_{star}	1	14	MΩ	
Ambient temperature range	T_{opr}	-40	85	℃	
Capacitance of FB pin	C_{FB}		2.2	nF	
Capacitance of CS pin	C_{CS}	47	390	pF	

DC Electrical Characteristics (VCC =15V, Ta=25°C)

Supply Voltage (VDD Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Startup Current	I_{DD-ST}		2	3	μA	VDD=15V
Operating Current (with 1nF load on DRV pin)	I_{DD-OP}	0.4	0.6	0.8	mA	V_{FB}=0V
	I_{DD-OP}	1	2	2.3	mA	V_{FB}=2.5V CL=1nF
	I_{DD-OLP}	0.2	0.35	0.5	mA	Protection Current
UVLO (off)	$V_{UVLO-OFF}$	7.5	8	8.5	V	
UVLO (on)	$V_{UVLO-ON}$	16		19	V	
VDD OVP Level	V_{OVP}	26	27	28.5	V	
OVP Debounce Time	T_{OVP}		4		cycle	Guarantee by Design
VDD Simulation mode(ON)	V_{DD-HD_ON}	9.7		10.7	V	
VDD Simulation mode(OFF)	V_{DD-HD_OFF}	10.2		11.2	V	
Latch off mode release Current	IDD_{-LHOFF}			25	uA	Guarantee by Design

Voltage Feedback(FB Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	I_{Zero}	0.1	0.14	0.18	mA	V_{FB}=0V
Open Loop Voltage	V_{FB-OP}	4.8	5	5.2	V	FB pin open
Over Load Protection	V_{OLP}	3.5	4	4.5	V	
Debounce Time of OLP	T_{OLP}	55	65	75	ms	
Burst mode start voltage(on)	V_{BUR_ON}	0.35	0.45	0.55	V	
Burst Mode Hysterics	V_{BUR_HY}	0.05	0.1	0.15	V	
Green Mode Threshold	F_{th_GR}	55	60	75	KHz	V_{FB}=1.3V

Current Sensing (CS Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time & Propagation Delay to Output	T_{LEB} +T_{PD}	400	500	600	ns	
Maximum CS Off Voltage	V_{CSTH}	0.65	0.7	0.75	V	
OCP source current	I_{OCP}	240	250	260	uA	Min. Duty
CS Over Voltage Protection	V_{CS_OVP}	0.45	0.5	0.55	V	T = T_{off}
OVP Leading Blanking time	T_{OVP_LEB}		2		us	Guarantee by Design
Internal Slope Compensation	$V_{SLP\_LP\_LEB}$		160		mV	
Short Circuit Protection Voltage	V_{SCP}		1		us	
Debounce Time of V_{SCP}	T_{SCP}		4		cycle	
Short Circuit Detection Time	T_{SCP}		100		us	

Alternating Current *Detect(AC Pin):*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Brown In trigger point	V_{BNI}	0.8	0.85	0.9	V	
Brown Out trigger point	V_{BNO}	0.65	0.7	0.75	V	
BNO De-bounce time	T_{BNO}	20	26.5	30	ms	

SDSP (Secondary diodes short protection):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
SDSP CS pin level	V_{CS_SDSP}		0.85		V	
De-bounce Cycle	T_{D_SDSP} (*)		2		Cycle	Guarantee by Design

Timer Section:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F_{Burst}	20	22.5	28	KHz	
PWM Mode Frequency	F_{PWM}	95	100	105	KHz	
Voltage stability of Frequency	F_{PSRR}	-1		+1	%	VDD = 11V~25V
Frequency Shuffling Range	F_{jitter}	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D_{MAX}	75	80	85	%	
Internal Soft Startup Time	T_{SS}	6.7	8.6	10.5	mS	

On chip OTP:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
OTP Level			150		℃	
OTP exit			120		℃	

650V MOSFET (Drain Pin) :

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark	Package
MOSFET Drain-source Breakdown Voltage	BV_{DSS}	VGS=0V ID=250uA	650			V		
		VGS=10V ID=0.5A		7.5	10	Ω	EST.3011MS	**SOP-8**
Static drain-source on-resistance	$RDS_{(on)}$	VGS=10V ID=0.5A		4.0	5.0	Ω	EST.3013MS	**SOP-8**
		VGS=10V ID=1A		2.5	3.5	Ω	EST.3015MS	**SOP-8**
		VGS=10V ID=0.5A		2.4	2.8	Ω	EST.3017MS	**SOP-8**
		VGS=10V ID=0.6A		1.8	2.2	Ω	EST.3019MS	**SOP-8**

700V MOSFET (Drain Pin) :

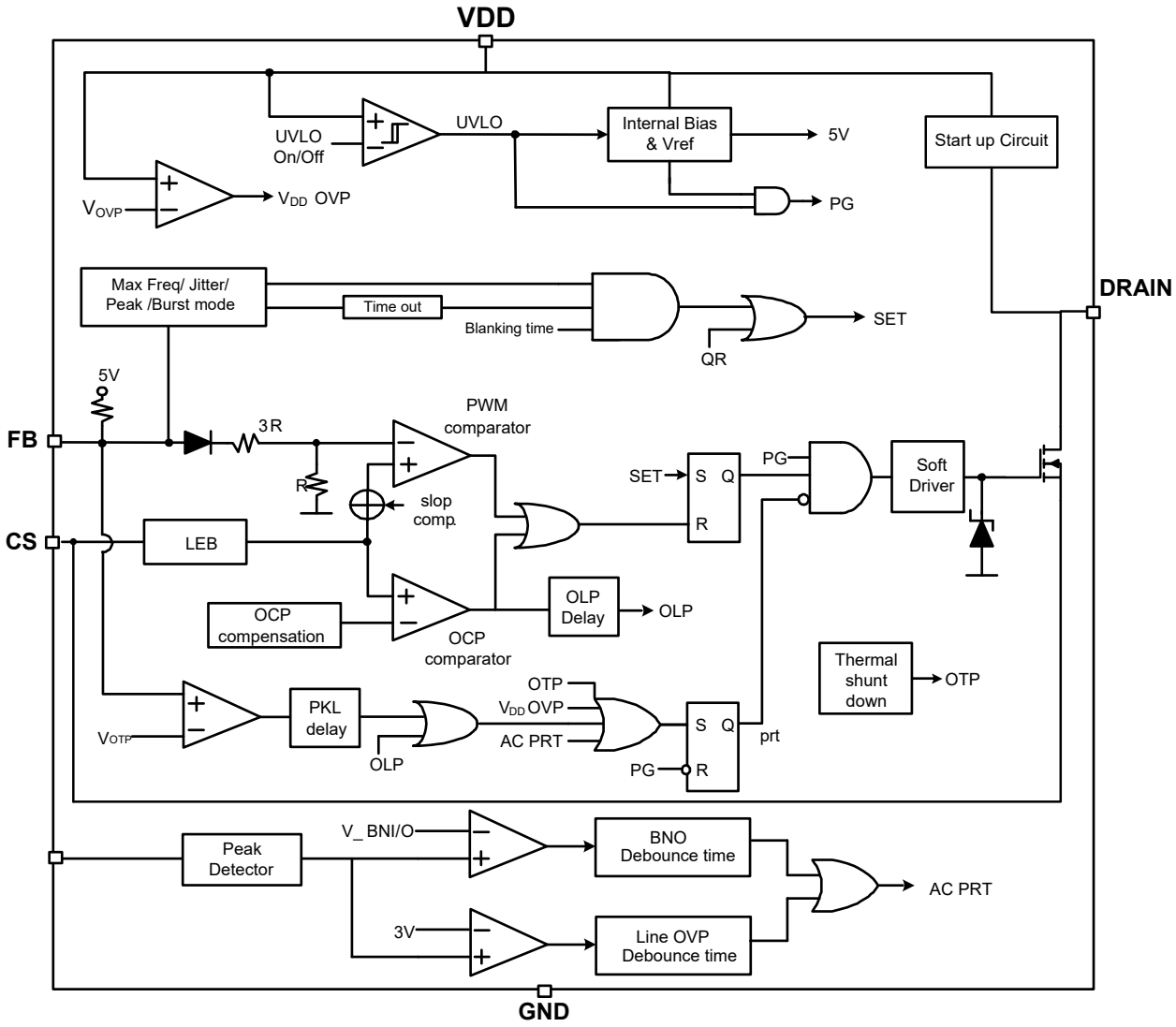
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark	Package
MOSFET Drain-source Breakdown Voltage	BV_{DSS}	VGS=0V ID=250uA	700			V		
Static drain-source on-resistance	$RDS_{(on)}$	VGS=10V ID=0.5A		13.0	14.5	Ω	EST.3021MS	**SOP-8**
		VGS=10V ID=1A		4.0	5.0	Ω	EST.3025MS	**SOP-8**
		VGS=10V ID=1.5A		3.6	4.2	Ω	EST.3027MS	**SOP-8**
		VGS=10V ID=2.0A		2.6	3.2	Ω	EST.3029MS	**SOP-8**

800V MOSFET (Drain Pin) :

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark	Package
MOSFET Drain-source Breakdown Voltage	BV_{DSS}	VGS=0V ID=250uA	800			V		
Static drain-source on-resistance	$RDS_{(on)}$	VGS=10V ID=1.5A		4.0	5.0	Ω	EST.3037MS	**SOP-8**

Block Diagram

EST.30xxMS



Application Note

Operation Overview

The EST.30xxMS meets the green power requirement and is very suitable for the application of those networking adaptors and the kinds of consumer power. It can provide more power efficiency conversion and keeps lower power loss. It also supports completely kind of protection for every abnormal environments.

SS，Soft-start Sequence

EST.30xxMS also builds up 8.6 ms (typical) soft-start to soften the electrical stress occurring in the power supply during startup, refer to Fig.2-3. As soon as VDD reaches UVLO _on, the Cs peak voltage is gradually increased from 0.2V to the maximum level.

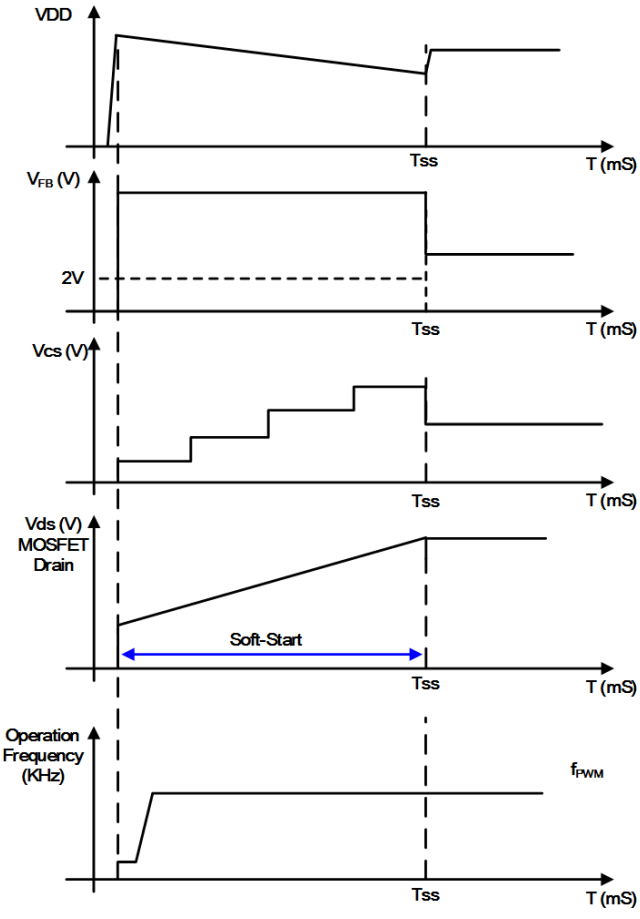


Fig.2-3

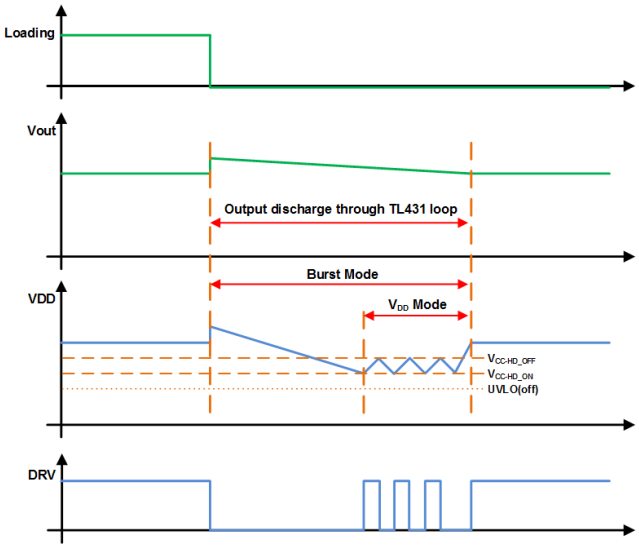
VDD Stimulation Mode

EST.30xxMS provides stimulation mode to avoid abnormal re-start-up under the situation of heavy loading to no-load, caused by non-balance of discharge of VDD cap and output cap, which is different with burst mode. The waveform is shown in fig.2-4

Condition : V_{FB} < V_{BUR_ON} & V_{DD} <9.5V trigger, Hysterics Voltage 1V

Action：IC fix output F_{Burst}, and V_{CS} keeps as 0.15V

Notice： Design $V_{\_AUX}$ higher than 11V



FB，Voltage Feedback Loop

EST.30xxMS uses current mode control, that is say, the voltage feedback signal is provided from TL431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

(1). R_{bias1} and R_{bias2} to prevent the abnormal output

voltage at heavy loading. Generally, we suggest R_{bias1} 100~1KΩ，R_{bias2} 1.5~2.5KΩ

(2). R_{phase}/C_{phase} is for RC phase compensation and prevent oscillate to adjust the value of C_{FB}

(3). Generally, we suggest R_{phase}1~10KΩ ，C_{phase} 0.1uF ，C_{FB} 1~2.2nF

(3). The ratio of R_3 and R_{3A} is depent on the output voltage spec (EST.431, V= 2.5V)

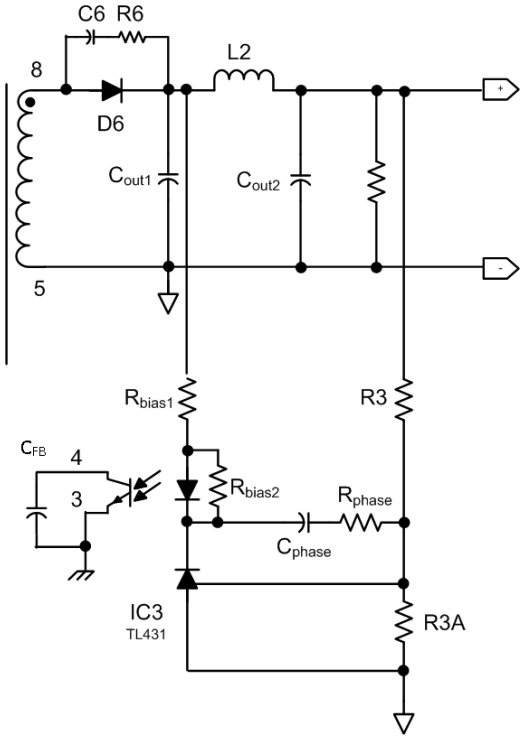


Fig.2-6

In addition, V_{FB} is also used to determine the green mode level .When V_{FB} is under V_{BUR_ON} , it is under no load or light load condition; at light loading, burst mode can effectively reduces the switching loss. When V_{FB} is larger than V_{BUR_ON}, it will leave away the standby mode. The normal operation of V_{FB} is from V_{BUR_ON} to 2.4V,; meanwhile, short-circuit current is around I_{Zero}.

CS, Current sense Loop

Current mode PWM control mode detects the current command (CS) from the Rsense (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continues conduction mode (CCM) , therefore, EST.30xxMS also builds in the slope compensation between high and low AC line to avoid the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS pin being damaged by the unknow negative spike.

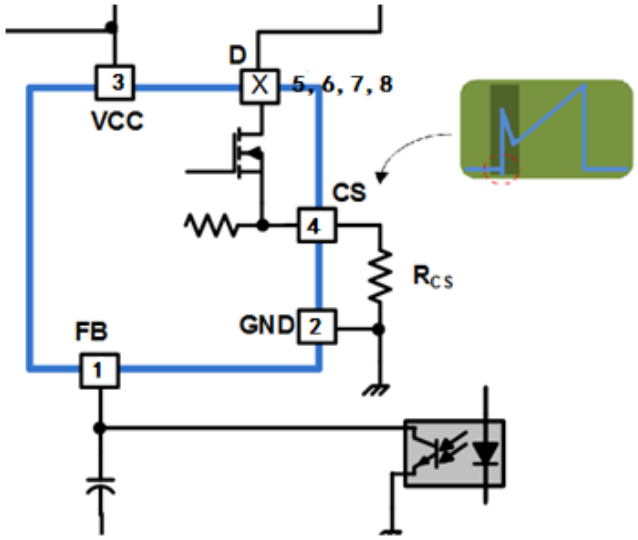


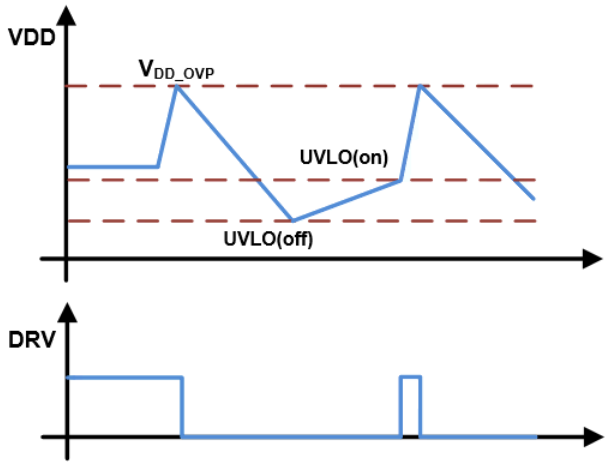
Fig.2-7

Complete Protection

EST.30xxMS integrates various kind of protection to make sure operation safety.

VDD OVP (Over Voltage Protection)

The maximum ratings of the EST.30xxMS are around 30V. To prevent the VDD enter breakdown condition, EST.30xxMS series are integrated with OVP function on VDD pin. Whenever the VDD voltage is higher than the V_{OVP} threshold, the output gate drive circuit will be turn-off simultaneously and the power MOSFET is turn-off until the next UVLO(on) cycle.



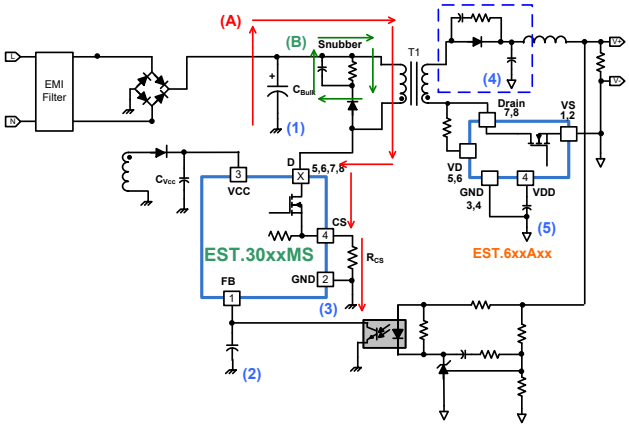


Fig.2-8

SDSP, Secondary Diode Short Protection

After short circuit of 2nd side schottky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high Vds to damage MOSFET.

EST.30xxMS detects the inductance current through the resistance, Rcs, of CS pin, and will trigger protection (latch or hiccup) when Vcs higher than 0.85V and sustains 2cycle timing.

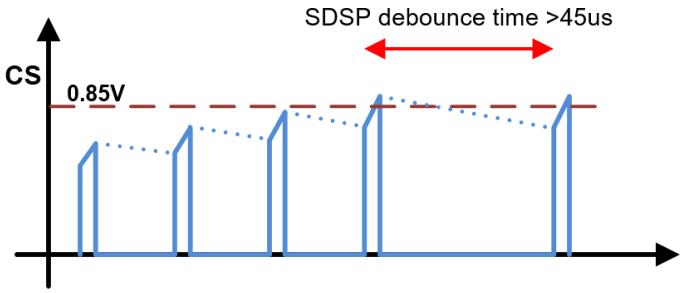


Fig.2-9

Layout Guide line

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

Big current path : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area

Low voltage area : R devider need to be as near FB_Pin as possible.

Secondary Side Schottky : routing as close as possible

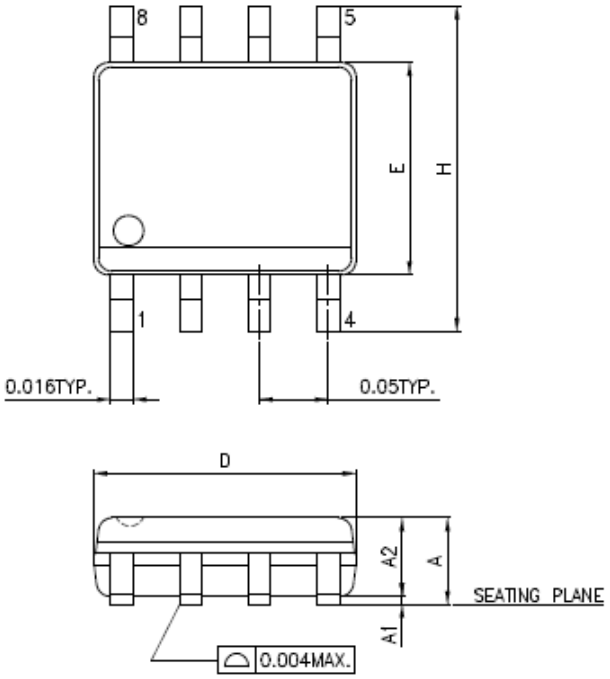
Grounding : (2) and (3) grounding separated with each other, and end connects to (1) ground.

Table 1: Complete Protection

Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VDD OVP	VDD	VDD > 26V
1st	V-Sense	VDD UVLO Off	VDD	VDD < 7.5V
1st	V-Sense	CS pin open	CS	V_{CS} >0.7V after 4 cycles
2nd	SDSP	2nd side Schottky short	CS	VCS >0.85V after 2 cycles
2nd	SCP	Output short	CS	1. 12ms blank time during start-up 2. after 4 cycles 3.Duty < 10%
2nd	OVP	Output OVP	CS	Vcs compares to 0.5V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS=0.7V
2nd	OLP	OLP	FB	CS > 4V
IC	Chip OTP			chip OTP at 150 ℃

Package Information

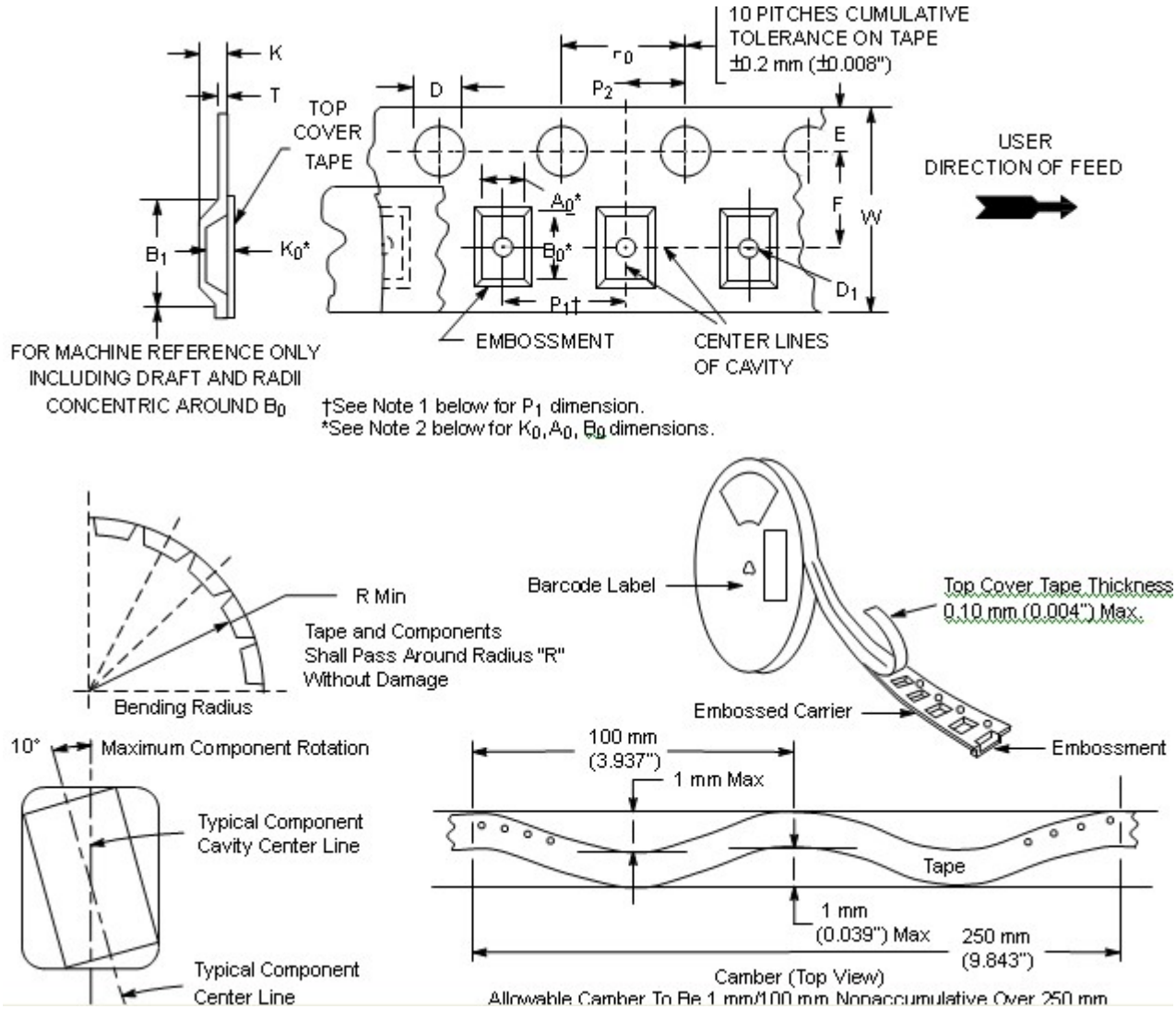
SOP-8 Package （mm）



Symbols	Dimensions In Inches			Dimensions In millimeters		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	0.050	0.061	0.072	1.270	1.549	1.829
A1	0.000	------	0.010	0.000	------	0.254
A2	------	------	0.062	------	------	1.575
D	0.185	0.193	0.200	4.699	4.902	5.080
E	0.147	0.154	0.160	3.734	3.912	4.064
H	0.225	0.237	0.249	5.715	6.020	6.325
L	0.013	0.033	0.053	0.330	0.838	1.346
θ	0°	4°	8°	0°	4°	8°

Embossed Tape and Reel Data Carrier Tape Specifications

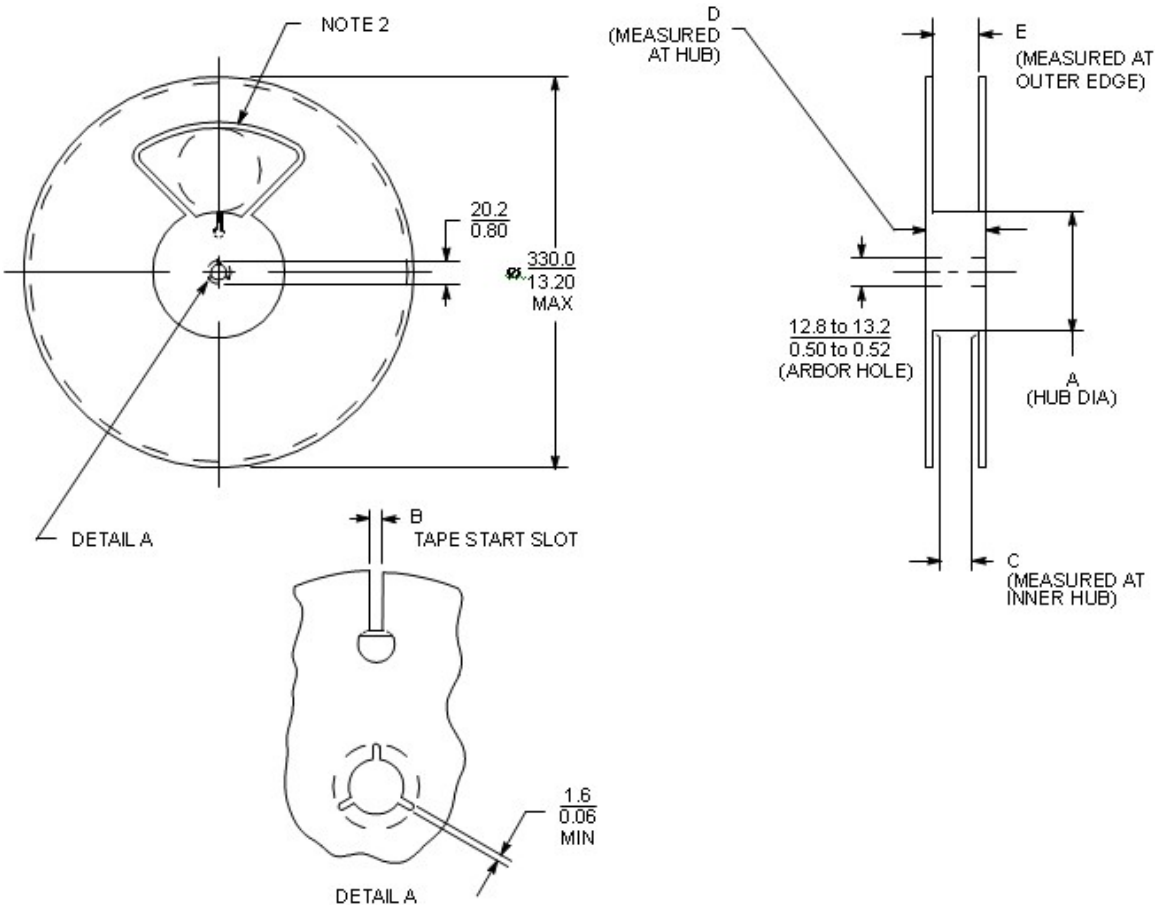
SOP-8/ Tape Reel Data



DIMENSIONS

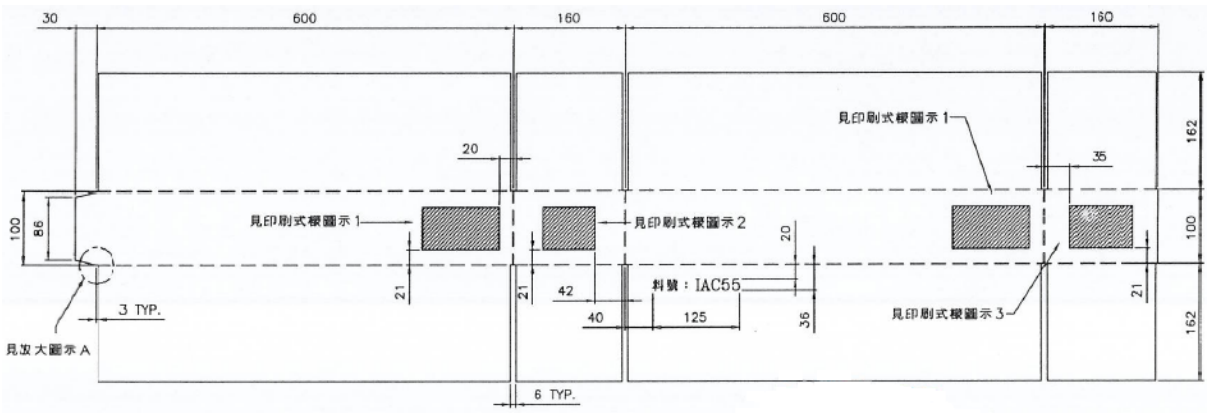
Tape ize (W)	B1 Max (Note 1)	D	D1	E	F	K	P0	P2	R Min	T Max	W Max
8 mm	4.55 mm (0.179″)	1.5 + 0.1 − 0.0 (0.059 + 0.004″ − 0.0)	1.0 Min (0.039″) or 0.5 mm Min (0.020″)	1.75 ± 0.1 (0.069 ± 0.004″)	3.5 ± 0.05 (0.138 ± 0.002″)	2.4 mm Max (0.094″)	4.0 ± 0.1 mm (0.157 ± 0.004″)	2.0 ± 0.1 mm (0.079 ± 0.002″)	25 mm (0.98″)	0.6 mm (0.024″)	8.3 mm (0.327″)
12 mm	8.2 mm (0.323″)		1.5 mm Min (0.060″)		5.5 ± 0.05 (0.217 ± 0.002″)	6.4 mm Max (0.252″)			30 mm (1.18″)		12 ± 0.30 (0.470 ± 0.012″)
16 mm	12.1 mm (0.476″)				7.5 ± 0.10 (0.295 ± 0.004″)	7.9 mm Max (0.311″)					16.3 mm (0.642″)
24 mm	20.1 mm (0.791)				11.5 ± 0.1 (0.453 ± 0.004″)	11.9 mm Max (0.468″)					24.3 mm (0.957″)

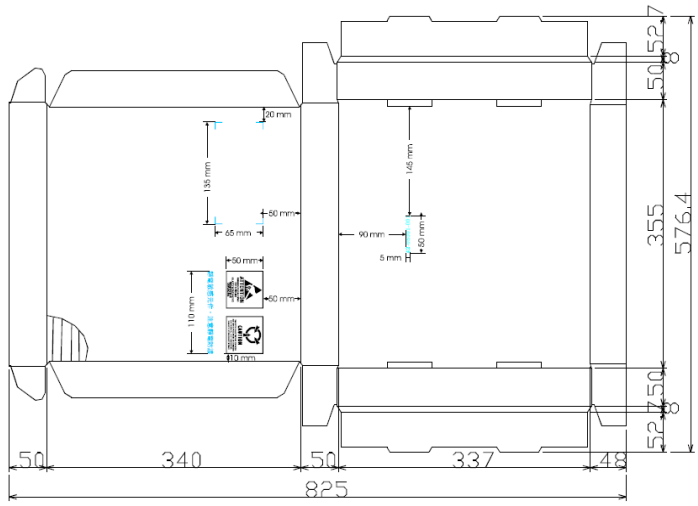
Reel Dimensions



Reel Diameter	Tape Size	A mm (inches)		B mm (inches)		C mm (inches)		D (Max)	E (Max)
		Min	Max	Min	Max	Min	Max		
178.0 (7.01)	16.0 (0.63)		50.0 (1.97)	6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)	178.0 (7.01)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	56.0 2.20	150.0 (5.91)		10.0 (0.39)	11.0 (0.43)	56.4 (2.22)	58.4 (2.30)	62.4 (2.46)	59.4 (2.34)
330.0 (12.99)	44.0 (1.73)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	44.4 (1.75)	46.4 (1.83)	62.4 (2.46)	47.4 (1.87)
330.0 (12.99)	32.0 (1.26)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	32.4 (1.28)	34.4 (1.35)	38.4 (1.51)	35.4 (1.39)
330.0 (12.99)	24.0 (0.94)	60.0 (2.36)		9.5 (0.37)	10.5 (0.41)	24.4 (0.96)	26.4 (1.04)	30.4 (1.51)	27.4 (1.08)
330.0 (12.99)	16.0 (0.63)			6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)			4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.01)	12.0 (0.47)	50.0 (1.97)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.47)	10.9 (0.43)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)

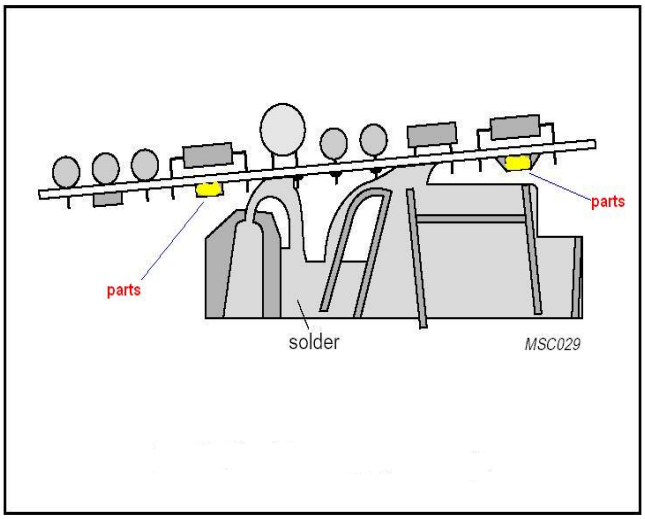
Tube Inner box Data

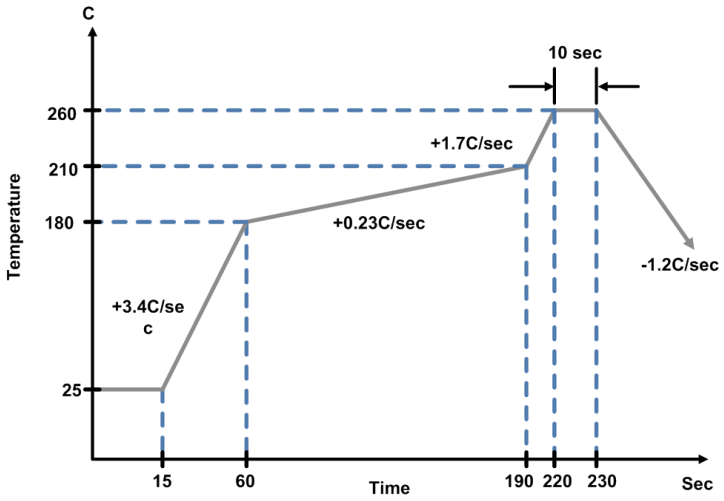




Reliability Test Program

Reflow Condition (IR/Convection or VPR Reflow)





Test Item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245℃, 5sec
HOLT	MIL-STD-883D-1005.7	1000Hrs Bias@125℃
PCT	JESD-22-B,A102	168Hrs, 100% RH, 121℃
TST	MIL-STD-883D-1011.9	-65℃~150℃, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHMB>2KV, VMM>200V
Latch-Up	JESD 78	10ms, 1_{tr}> 100mA

Revision History

REVISION	DESCRIPTION	PAGE	DATE
Rev 1.0	First release	13	2021/05/10