Data Sheet

Type Description :	**High Voltage Green-Mode PWM Flyback (SSR) Controller**
Product Name :	**EST.3000xS**
Reversion :	**V1.0**
Reversion Date :	**May, 2019**
Page :	**16 Pages**

General Description

The EST.3000xS is a series of high-performance current mode PWM controllers with integrated high-voltage device provides fast start-up function without external start-up resistors.

The EST.3000xS also integrates the intelligent zero-watt mode (ZWMTM)technology, which technology can provides an excellent green power solution, especially under light-load and no-load conditions.

It also features brown-in and brown-out detection.

The EST.3000xS offers complete protection functions such as internal Over-Temperature Protection (OTP), Over-LoadProtection (OLP) and VDD Over-Voltage Protection (OVP).

It also features Secondary Rectifier Short-circuit

Protection (SCP1) 、Cable end short-circuit Protection(SCP2) and Current Sensing pin (CS) open circuit

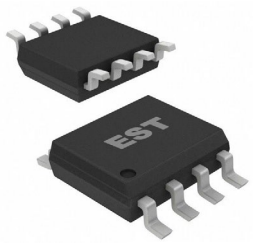
protection. Due to these protections, design of power supply unit becomes simple and reliable.

The EST.3000xS provides several versions, shown in the version table, for various applications.

X is for function options

Features

- Integrated 700V Start-Up Device
- Brown-In and Brown-Out
- X-cap discharge
- Low No-Load Input Power (<30mW)
- Accurate Over Load Protection
- Driver Capability : 400mA/−400mA
- RTL pin for Arbitrary External Protection
- Zero Watt Mode (ZWMTM) for 10mW Solution
- Jittering Frequency
- Soft Driving for Reducing EMI Noise
- VDD Over Voltage Protection
- Internal Over Temperature Protection
- Secondary Rectifier Short Protection
- Cable-end Short Protection
- CS Pin Open Protection
- RoHS Compliant and Halogen Free



SOP-8L

Application

- Switching AC/DC adapter and battery charger
- ATX standby power
- Open frame switching power and CD(R)
- Set-top-boxes(STB) 384Xreplacement

Function and Protection Options

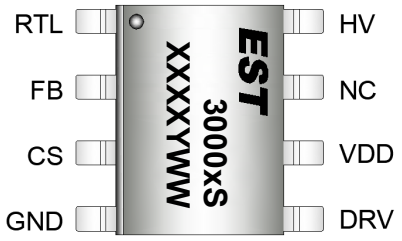
Part No.	Package	Freq.	Protection							
		KHZ	VCC OVP	OLP (65mS)	AUX. OVP	AUX. UVP	CS Open	SDSP	Line OVP	BNO
EST.3000AS	SOP-8L	65KHz	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup
EST.3000RS	SOP-8L	65KHz	Latch	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup
EST.3000LS	SOP-8L	65KHz	Latch	Latch	Latch	Latch	Hiccup	Hiccup	Hiccup	Hiccup

Note: EST lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. EST lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. EST defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

Ordering Information

Part Number	Package	Packaging	Note
EST.3000AS & ASR	SOP-8L	Tape & Reel	Green
EST.3000RS & RSR	SOP-8L	Tape & Reel	Green
EST.3000LS & LSR	SOP-8L	Tape & Reel	Green

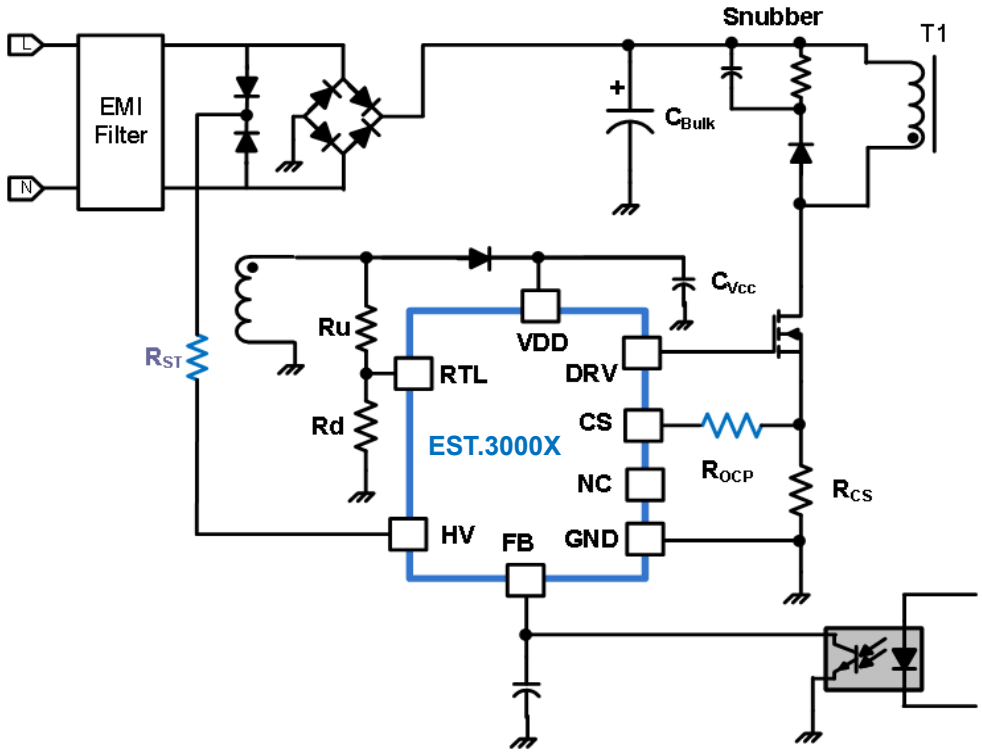
Pin Assignments and Package Type



EST: LOGO
XXXX: Production lot code
Y: Year code
WW: Week code

SOP-8L	NAME Description	Description
1	RTL	External Protection Input for Output OVP or Line OVP
2	FB	Feedback Voltage Input. Connect an opto-coupler to close the control loop and achieve output voltage regulation.
3	CS	Current Sense Input. The current sense resistor between this pin and GND is used for current limit setting.
4	GND	Ground of the Controller.
5	DRV	Gate Driver Output for the External MOSFET.
6	VDD	Supply Voltage Input. The controller will be enabled when VDD exceeds UVLO_ON and disabled when VDD decreases lower than UVLO_OFF.
7	NC	
8	HV	High Voltage Input for Start-Up. AC Brown in/out and Line OVP detection.This pin can withstand high voltage up to 700V.

Application Circuit



Absolute Maximum Ratings

Parameter Symbol		Symbol	Limit Values		Unit	Remark
			Min.	Max		
Supply Voltage VDD		V_{DD}	-0.3	30	V	
FB,CS,RTL		V_{FB} V_{CS} V_{RTL}	-0.3	7	V	
HV to GND		V_{HV}	-0.3	700		
Gate Driver Voltage		V_{DRV}	-0.3	V_{DD}+0.3	V	
Gate Output Current		I_{DRV}		500	mA	
Operation Junction Temperature		Tj	-40	150	℃	
Operation Ambient Temperature		T_A	-25	85	℃	
Storage Temperature		T_{stg}	-55	150	℃	
Power Dissipation @TA=85℃		P_D	-	220	mW	
Junction-to-Ambient Thermal Resistance*	Ta = 25℃	θ_{JA}		180	℃/W	SOP-8
Junction-to-Case Thermal Resistance**	Ta = 25℃	θ_{JC}		39	℃/W	
Lead temperature (Soldering, 10 sec)			-	260	℃	
ESD Voltage Protection	HBM	$V_{ESD-HBM}$	-	3.0	KV	
	MM	V_{ESD-MM}	-	300	V	

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
Supply Voltage VDD	V_{DD}	10	26	V	
Supply Voltage HV	V_{HV}		700	V	
Startup Resistor Value	Rstar	265	300	KΩ	
Junction temperature range	Tj	-40	150	℃	
Ambient temperature range	Topr	-40	85	℃	
Capacitance of FB pin	C_{FB}		2.2	nF	

DC Electrical Characteristics (VCC =15V, Ta=25°C)

HV Section (VHV Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
IHV Supply Current for HV pin	I_{HV-ST1}		20		mA	VDD < UVLO ON, V_{HV}=200V
Off State Leakage Current	I_{HV-LK}		1		μA	VDD > UVLO ON, V_{HV}=560V
X-cap Discharge De-bounce Time	$T_{Xcap-dis}$		64		mS	Freq. = 65KHz
Brown In trigger point	V_{BNI}	81	85	89	V	R_{ST} = 281KΩ
Brown Out Hysteresis Voltage	V_{BNO}	10	15	20	V	R_{ST} = 281KΩ
BNO De-bounce time	T_{BNO}	16	21	33	mS	
Line OVP trigger point	V_{LNOVP}	300	315	330	V	R_{ST} = 281KΩ
Line OVP Hysteresis Voltage	V_{LNOVP_HYS}	10	15	20	V	R_{ST} = 281KΩ
Line OVP De-bounce time	T_{LNOVP}	130	140	150	mS	
AC detect time	T_{ACD}	20	22.5	25	mS	

Supply Voltage (VCC Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Current (with 1nF load on DRV pin)	I_{CC-OP}	0.4	0.6	0.8	mA	V_{FB}=0V
	I_{CC-OP}	1.5	2	2.5	mA	V_{FB}=2.5V CL=1nF
	I_{CC-OLP}	0.2	0.35	0.5	mA	Protection Current
UVLO (off)	$V_{UVLO-OFF}$	7.5	8	8.5	V	
UVLO (on)	$V_{UVLO-ON}$	17	18	19	V	
VDD OVP Level	V_{OVP}	26	27	28	V	
OVP Debounce Time	T_{OVP}		4		cycle	Guarantee by Design
VDD Simulation mode(ON)	VDD_{-HD_ON}	9.7	10.2	10.7	V	
VDD Simulation mode(OFF)	VDD_{-HD_OFF}	10.2	10.7	11.2	V	

Voltage Feedback(FB Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	I_{Zero}	0.1	0.14	0.18	mA	V_{FB}=0V
Open Loop Voltage	V_{FB-OP}	4.8	5	5.2	V	FB pin open
Burst mode start voltage(on)	V_{BUR_ON}	0.9	1	1.1	V	RTL Discharge Voltage 2.7 *
Burst Mode Hysterics	V_{BUR_HY}	0.05	0.1	0.15	V	
Green Mode Threshold	V_{th_GR}		1.5		V	
Green Mode End Threshold	$V_{th\_GR\_end}$		1.1		V	

Current Sensing (CS Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time & Propagation Delay to Output	$T_{LEB}+T_{PD}$	300	400	500	ns	
Maximum CS Off Voltage	V_{CSTH}	0.65	0.7	0.75	V	
OCP source current	I_{OCP}	18.5		21.5	%	I_{OCP}/I_{AUX}
Over Load Protection	V_{OLP}	0.45	0.5	0.55	V	T_{ON}
Debounce Time of OLP	T_{OLP}	54	64	74	mS	
Over temperature protection	V_{OTP}	0.45	0.5	0.55	V	T_{OFF}
Debounce Time of OTP	T_{OTP}	54	64	74	mS	
OTP Leading Blanking time	T_{OTP_LEB}		2		uS	Guarantee by Design
Short Circuit Protection Voltage	V_{SCP}		0.85		V	
Debounce Time of V_{SCP}	T_{SCP}		3		cycle	

Miltiple function (RTL Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output OVP Trigger Point	V_{TH_OVP}	2.9	3	3.1	V	FB>4V
Output OVP Deglitch Time Constant	$T_{\_OVP\_delay}$		4		Cycle	Guarantee by Design
Output UVP Trigger Point	V_{TH_UVP}	0.7	0.8	0.9	V	FB>4V
Output UVP Deglitch Time Constant	$T_{\_OVP\_delay}$		4		Cycle	Guarantee by Design
Positive Clamped voltage	V_{POS}	6		7	V	
Negative Clamped voltage	V_{NEG}	-0.05		0.05	V	
RTL Leading Blanking time	T_{RTL_LEB}		*2*		*uS*	Guarantee by Design

Driver(DRV Pin) :

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output Low Level	V_{OL}			1	V	VDD = 16V, IO=20mA
Output High Level	V_{OH}	8			V	VDD = 16V, IO=20mA
Output Clamp Voltage Level	V_{G_Clamp}	11	12.5	14	V	VDD = 25V
Rising Time	T_R	200	300	400	nS	VDD = 16V, CL= 1nF
Falling Time	T_F	10	30	50	nS	VDD = 16V, CL= 1nF

Timer Section:

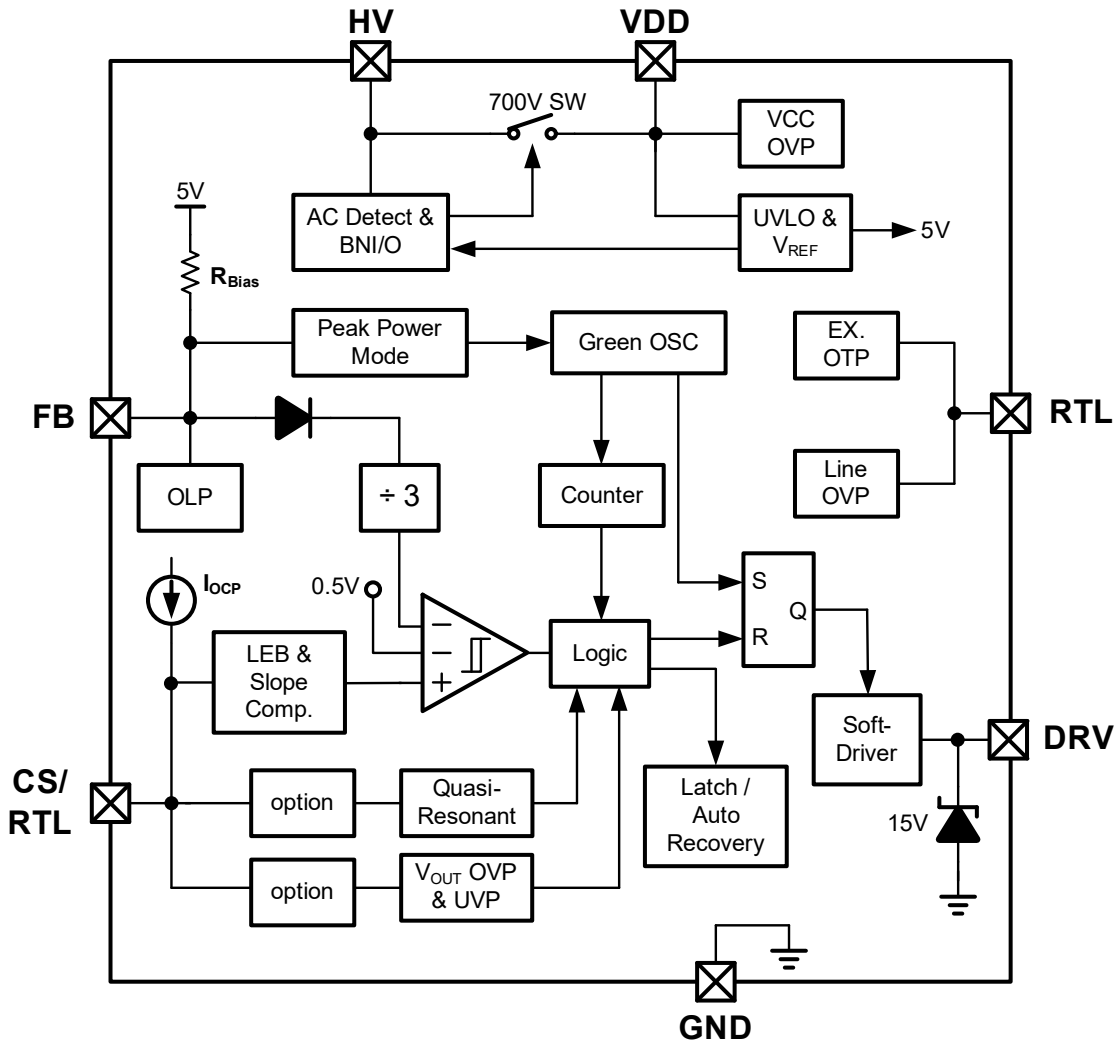
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F_{Burst}	20	22.5	25	KHz	
PWM Mode Frequency	F_{PWM}	61	65	69	KHz	
Voltage stability of Frequency	F_{PSRR}	-1		+1	%	VDD = 11V~25V
Frequency Shuffling Range	F_{jitter}	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D_{MAX}	75	80	85	%	
Internal Soft Startup Time	T_{SS}	10		15	mS	

On chip OTP:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
OTP Level			150		℃	
OTP exit			120		℃	

Block Diagram

EST.3000xS



Application Note

Operation Overview

The EST.3000xS meets the green power requirement and very suitable for the use in those networking adaptors ,TV open frame and various consumer power, which can provide more power efficiency and lower power loss. It also supports various kind of protection for every abnormal environments.

SS，Soft-start Sequence

EST.3000xS also built-up 12.5ms (typical) soft-start to soften the electrical stress occurring in the power supply during startup, refer to Fig.1. As soon as VDD reaches UVLO_on, the Cs peak voltage is gradually increased from 0.2V to the maximum level, see fig.1.

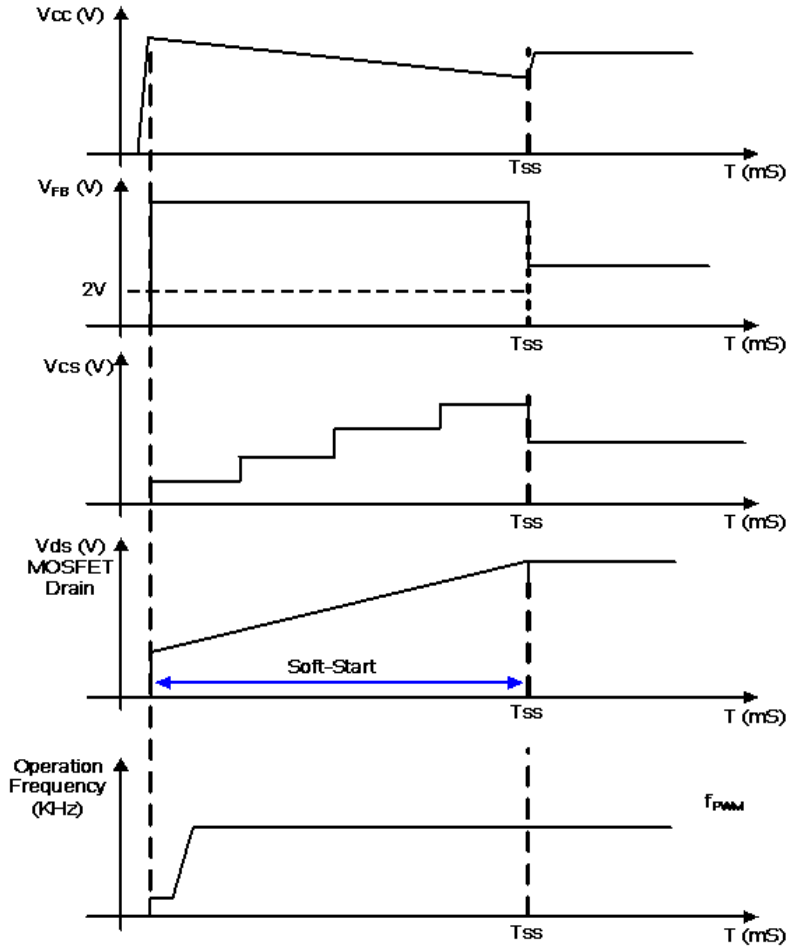


Fig.1

VDD Stimulation Mode

EST.3000xS provides stimulation mode to avoid abnormal re-start-up under heavy loading to no-load, caused by non-balance of discharge of VDD cap and output cap, which is different with burst mode. The waveform is shown in fig.2.

Condition：V_{FB} < V_{BUR_ON} & $_{VDD}$ <9.5V trigger, Hysterics Voltage 1V

Action：IC fix output F_{Burst} , and V_{CS} keeps as 0.15V

Notice： Design $V_{\_AUX}$ higher than 11V

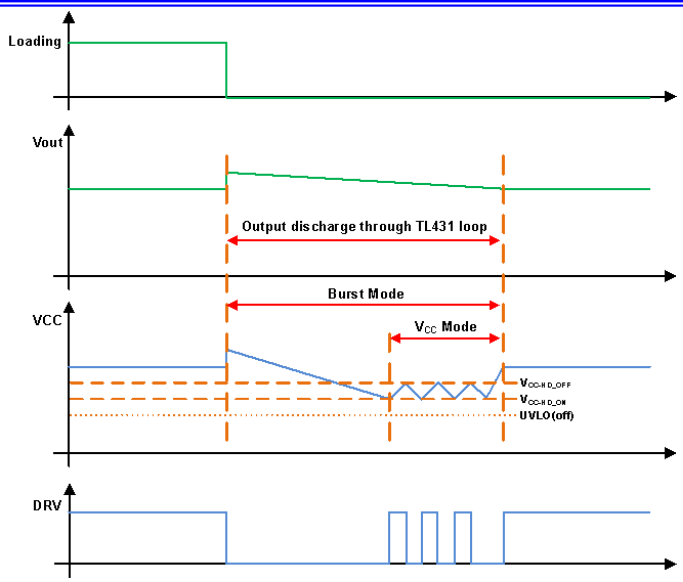


Fig.2

OLP (Over Load Protection)

EST.3000xS has new OLP built-in at CS pin, and its merit of close loop methodology makes audio noise free.

The adjustment of OCP is through RTL and CS, please refer to Fig.3. It can detect the status of AC line and output voltage through the resistance divider (Ru,Rd) by the reflection waveform of Aux-winding. At negative cycle, V_{RTL} will keep "0" and output I_{OCP} at CS pin to change the level of slope compensation, please see Fig.3. Therefore, it can modify the Ru and R_{OCP} to get target of OCP @full range.

Step 1. Sett R_U=200KΩ , Rd=39KΩ (initial setting) & R_{OCP} = 1KΩ and modifies R_{CS} to target of OCP@90Vac

Step 2. Increase R_{OCP} impedance to reduce OCP and check the OCP of AC full range. Modifies R_{OCP} to make OCP unanimous for AC full range.

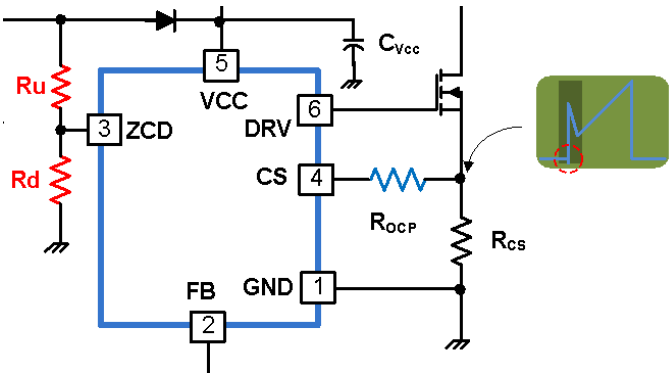


Fig.3

RTL : Demagnetization Detection from RTL pin (QR Mode Detection)

After MOSFET turns off, the current of secondary side diodes goes down to zero , and then the transformer core will be demagnetized completely, see fig.4. At the same time, a quasi resonant signal will be detected from auxiliary winding by RTL pin through the external resister divider.

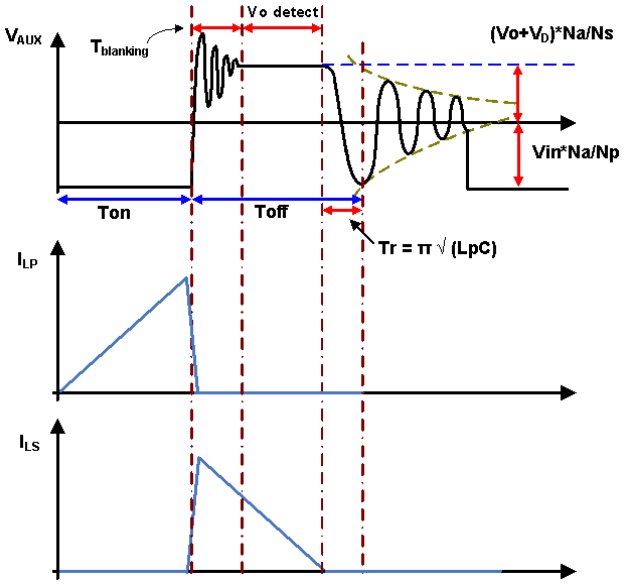


Fig.4

Programmable V_{O_OVP} & burst mode level

This RTL pin is also used to program the burst level at light load and high output voltage at system open loop . A resistive divider between Aux winding and GND is used to set a voltage at this pin to determine the peak current level when power entries the adaptive burst mode. At the same time, it also detects voltage level of output.

V_{O_OVP}：

Modifies R_d to target of V_{O_OVP}

Calculate the ratio of R_d to (R_u+R_d)

$$R_u = 200Kohm;$$

$$\frac{R_d}{R_u + R_d} = \frac{V_{TH\_OVP}}{(V_{O\_OVP} + V_d)} \times \frac{N_s}{N_a}$$

Adjust Burst：

$$V_{BUR\_ON} = (V_O + V_d) \times \frac{N_a}{N_s} \times \frac{R_d}{R_u + R_d} - 1.7$$

FB，Voltage Feedback Loop

EST.3000xS series adopt current mode control, that is say, the voltage feedback signal is provided from TL431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

(1). R_{bias1} and R_{bias2} to prevent the abnormal output voltage at heavy loading. Generally, we suggest R_{bias1} 100~1KΩ，R_{bias2} 1.5~2.5KΩ；

(2). R_{phase}/C_{phase} is for RC phase compensation and prevent oscillate to adjust the value of C_{FB}

(3). The ratio of R_3 and R_{3A} is depent on the output voltage spec (TL431 ,V= 2.5V)

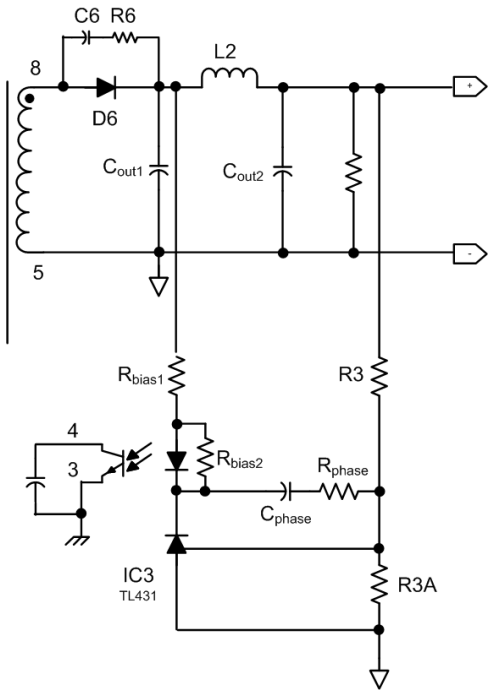


Fig.5

In addition, V_{FB} is also used to determine the green mode level .When V_{FB} is under V_{BUR_ON} , it is under no load or light load condition; at light loading, burst mode can effectively reduces the switching loss. When V_{FB} is larger than V_{BUR_ON}, it will leave away the standby mode. The normal operation of V_{FB} is from V_{BUR_ON} to 2.4V,; meanwhile, short-circuit current is around I_{Zero}.

CS, Current sense Loop

Current mode PWM control mode detects the current command (CS) from the Rsense (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continues conduction mode (CCM) , therefore, EST.3000xS series of built-in high and low slope compensation to avoid the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS pin being damaged by the unknow negative spike.

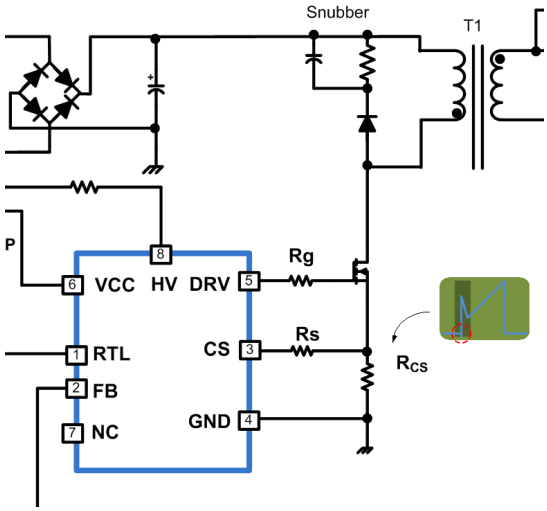


Fig.6

OTP (Over Temperature Protection on CS)

EST.3000xS is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As V_{CS} is greater than 0.5V and continues for 64ms，CS_OTP is triggered, than EST.3000xS is in protection mode till the temperature drops to setting work condition.

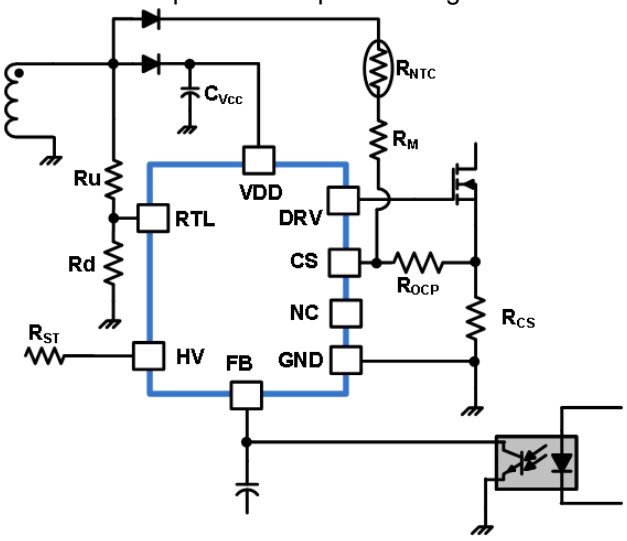


Fig.7

DRV

The driving capability of EST.3000xS is around 450mA, which can support power rate around 60~70W, and it is limited the maximum duty-cycle below 80% to avoid the transformer saturation.

Typically, the threshold of MOSFET is about 20V, and the maximum clamp voltage of EST.3000xS is 14V to prevent breakdown of MOSFET.

Complete Protection

EST.3000xS integrates various kind of protection to make sure operation safety.

VDD OVP (Over Voltage Protection)

The maximum ratings of the EST.3000xS are around 30V. To prevent the VDD enter breakdown condition, EST.3000xS series are integrated with OVP function on VDD pin. Whenever the VDD voltage is higher than the V_{OVP} threshold, the output gate drive circuit will be turn-off simultaneously and the power MOSFET is turn-off until the next UVLO(on) cycle.

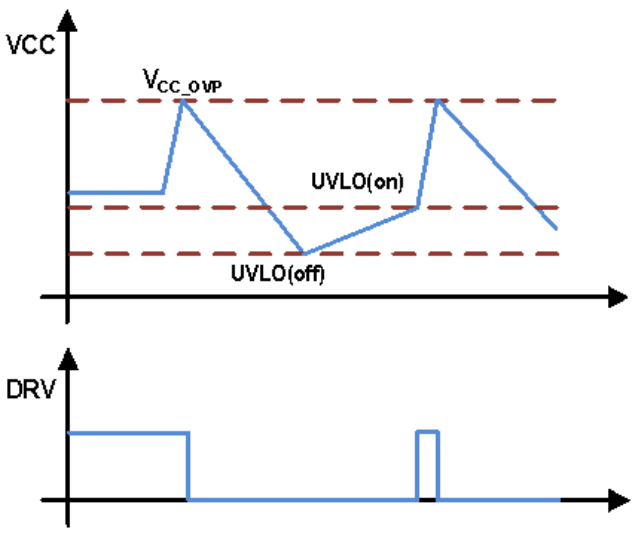


Fig.7

SCP (Short Circuit Protection)

A resistive divider between Aux winding and GND is used to monitor output voltage. When output circuit is short, Therefore, as V_{RTL} is lower than 0.8V during date off region, then V_{TH_UVP} is triggered, EST.3000xS is to enable UVP function in order to reduce input power

SDSP, Secondary Diode Short Protection

After short circuit of 2nd side schottky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high Vds to damage MOSFET. EST.3000xS detects the inductance current through the resistance, Rcs, of CS pin, and will trigger protection (latch or hiccup) when Vcs higher than 0.85V and sustains 3cycle timing.

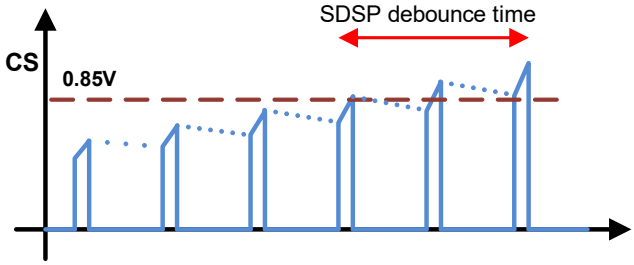


Fig.8

AC, Brown-in/out & Line OVP

EST.3000xS provides real detection of AC line through AC pin connected directly to AC line. When the VDD of EST.3000xS reaches UVLO_ON , it is into the state of
AC detection , and sustains a delay time T_{ADC} .

This AC pin is used to program the AV over and under voltage level through a resistive divider (Ra1/Ra2). If Vac is lower than below V_{BNI} or higher than V_{LNOVP_HYS},
It will turn-off the output till next cycle to check the condition is removed or not. Even after it turn-off, this pin is continues to detect line status. If Vac is lower than below V_{BNO} or higher than V_{LNOVP} for the timing T_{BNO} and T_{LNOVP}, it will be turn-off , and re-start again. Please refers to fig9.

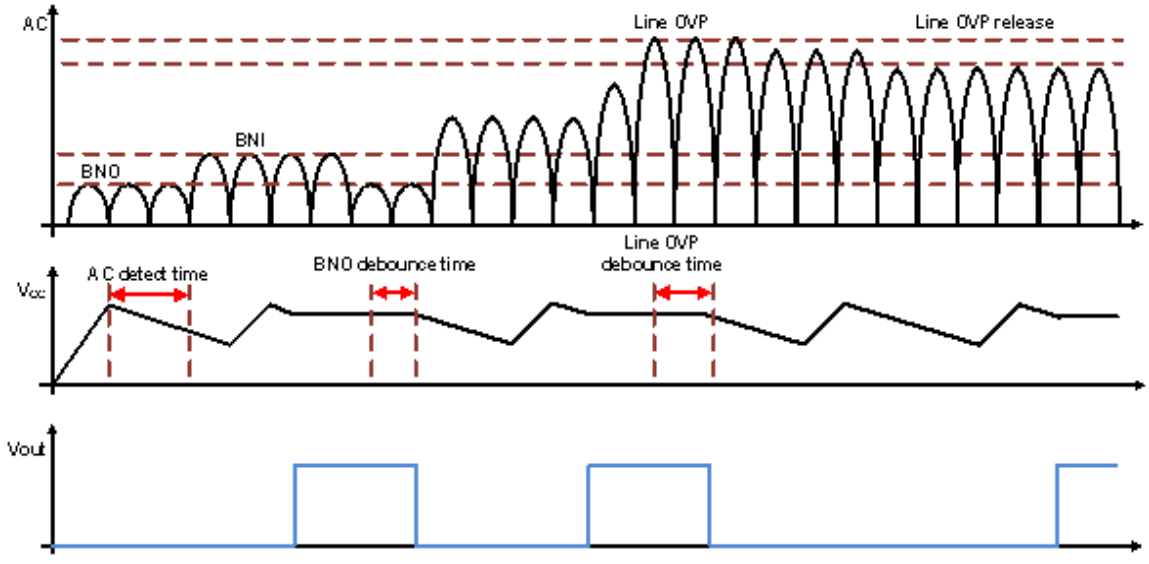
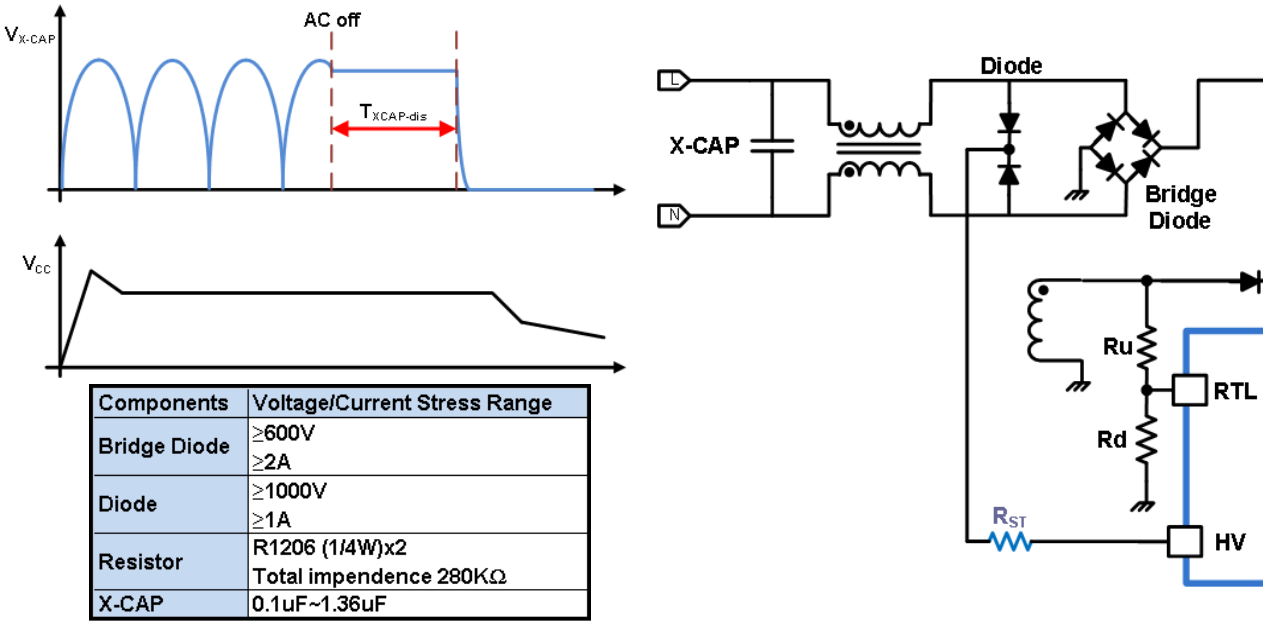


Fig.9

Intelligent AC off Detect with X-CAP discharge

The HV pin is also used for AC detection. When AC is off, the AC off state can be detected through HV pin. Then IC will provide a discharge path from HV pin to GND for the X-CAP discharge.



Components	Voltage/Current Stress Range
Bridge Diode	≥600V ≥2A
Diode	≥1000V ≥1A
Resistor	R1206 (1/4W)x2 Total impendence 280KΩ
X-CAP	0.1uF~1.36uF

Fig.10

Layout Guide line

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

- ✓ **Big current path** : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area
- ✓ **Low voltage area :** R devider need to be as near FB_Pin as possible.
- ✓ **Secondary Side Schottky :** routing as close as possible
- ✓ **Grounding :** (2).(3) and (4) grounding separated with each other, and end connects to (1) ground.
- ✓ **RTL :** Ru & Rd as close as possible to avoid noise coupling to trigger OVP.

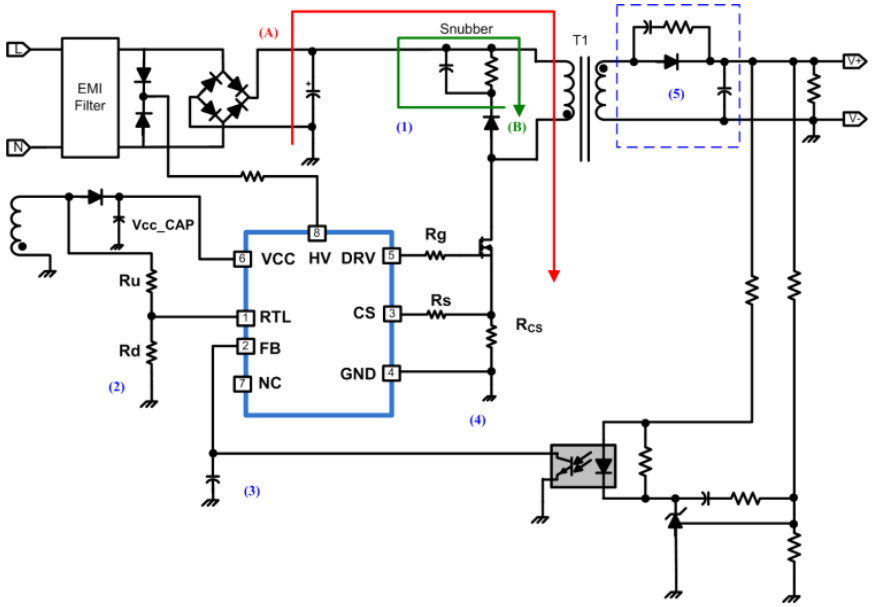


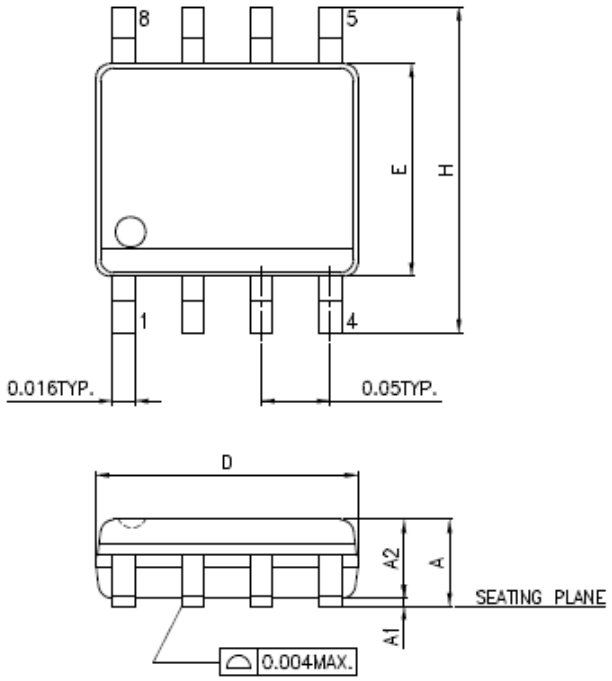
Fig.11

Table 1: Complete Protection

Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VCC OVP	Vcc	Vcc > 28V
1st	V-Sense	VCC UVLO Off	Vcc	Vcc < 7.5V
1st	V-Sense	Brown In Fail	AC	V_{AC}<0.85
1st	V-Sense	Brown out	AC	V_{AC}>0.75V
1st	V-Sense	Line OVP	AC	V_{AC}>3.0V
1st	V-Sense	T1 Aux gnd open	ZCD	ZCD UVP trigger
1st	V-Sense	MOS short/Gate to GND	ZCD	ZCD UVP trigger
1st	V-Sense	CS pin open	CS	V_{CS} >0.7V after 4 cycles
1st	ZCD	ZCD upper R open	ZCD	ZCD UVP：after soft-start ZCD<0.85V & FB>4V
1st	ZCD	ZCD upper R short	ZCD	ZCD OVP : ZCD>3V & FB>4V
1st	ZCD	ZCD down side open	ZCD	ZCD OVP : ZCD>3V & FB>4V
1st	ZCD	ZCD down-side short	ZCD	ZCD UVP：after soft-start time ZCD<0.85V & FB>4V
2nd	SDSP	2nd side Schottkey short	CS	VCS >0.85V after 4 cycles
2nd	SCP	Output short	ZCD	1. 12ms blank time during start-up 2. after 4 cycles 3. ZCD UVP = 0.8V & FB>4V trigger
2nd	OVP	Output OVP	ZCD	V_{ZCD} compares to 3V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS=0.7V
2nd	OLP	OLP	CS	CS > 0.5V
2nd	Short before power on		ZCD	1. 12ms blank time at start-up 2. after 4 cycles 3. ZCD UVP = 0.8V & FB>4V trigger
2nd	Short after power on		ZCD	1. after 4 cycles 2. ZCD UVP = 0.8V & FB>4V trigger
IC	Chip OTP			chip OTP at 150 ℃

Package Information

SOP-8 Package （mm）



Symbols	Dimensions In Inches			Dimensions In millimeters		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	0.050	0.061	0.072	1.270	1.549	1.829
A1	0.000	------	0.010	0.000	------	0.254
A2	------	------	0.062	------	------	1.575
D	0.185	0.193	0.200	4.699	4.902	5.080
E	0.147	0.154	0.160	3.734	3.912	4.064
H	0.225	0.237	0.249	5.715	6.020	6.325
L	0.013	0.033	0.053	0.330	0.838	1.346
θ	0°	4°	8°	0°	4°	8°