

## Data Sheet

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**Type Description :** Green-Mode PWM Controller (SSR)

**Product Name :** EST.28xxDR

**Reversion :** V1.1

**Reversion Date :** May, 2020

**Page :** 13 Pages

### General Description

EST.28xxDR is a higher integrated PWM flyback controller. It provides several functions to enhance the efficiency to meets the criteria of global standards such as DoE Level VI and EU CoC V5 Tier-2. Meantime, it also provides excellent EMI-improved solution, and also built in complete protection.

EST.28xxDR is a green mode controller, which implements low start-up current, green-mode power-saving. It is also built-in the leading-edge blanking (LEB) of the current sensing and feedback loop to screen the spike noise from any input signal. The internal slope compensation can limit the constant output over universal AC input range. The sawtooth over frequency function for EMI improved solution.

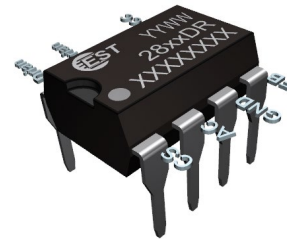
Meanwhile, EST.28xxDR also provides various protection, such as, OLP (Over Load Protection), VDD OVP (Over Voltage Protection), Output OLP and output OVP to prevent the circuit damage from the abnormal conditions.

EST.28xxDR is available in DIP-7.

EST.28xxDR works with current sensing synchronous rectifier controllers, such as EST.6001C and EST.6xxAxx to achieve higher conversion efficiency and very compact power density..

### Features

- Integrated high voltage MOSFET
- 65KHz fix frequency mode at PWM Mode
- Very low startup current (<3 uA)
- 0.5mA ultra-low operating current at light load
- Current mode control with Cycle-by-Cycle current limit
- Built-in slope and load regulation compensation
- LEB (Leading-edge blanking) on CS Pin
- UVLO (Under voltage lockout)
- Fault Protections : VDD Over Voltage, CS OVP(Over Voltage), Output Short-Circuit, Over-Current, OLP (Over load protection) and Pin Fault
- Photo coupler short protection & Feedback open protection
- High voltage CMOS process with excellent ESD protection
- 250mA/500mA driving capability
- Hazardous Substance Free
- RoHs/REACH Compliant



DIP-7L

### Application

- Switching AC/DC adapter and battery charger
- ATX standby power
- Open frame switching power and CD(R)
- Set-top-boxes(STB) 384Xreplacement

### Function and Protection Options

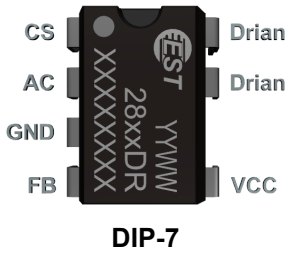
Part No.	Package	Freq. KHZ	Protection							
			OLP	BNO	VDD. OVP	AUX. OVP	CS. OVP	CS. Open	SDSP	
EST.28xxDR	DIP-7	65KHz	Hiccup / 100mS	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup	Hiccup

Note: EST lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. EST lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. EST defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

### Ordering Information

Part Number	Package	Packaging	Note
EST.28xxDR	DIP-7L	Tape	Green

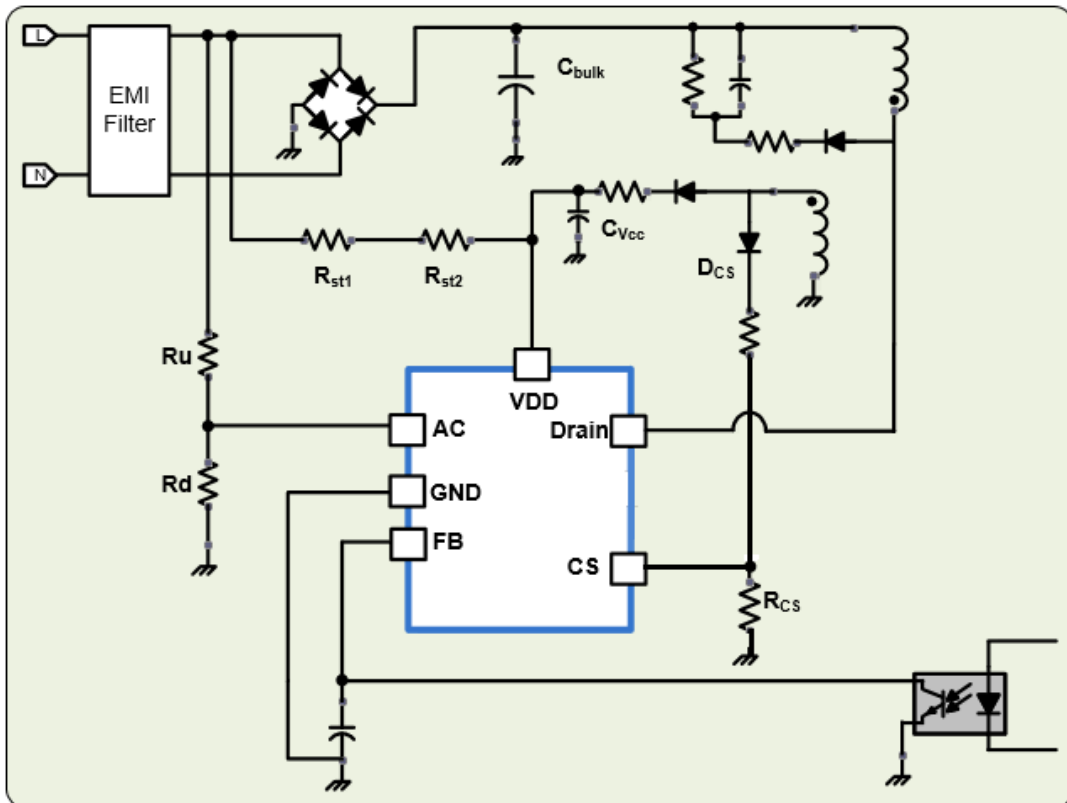
**Pin Assignments and Package Type**



EST: LOGO  
 YYWW: Date code  
 28xxDR: xx=MOS Type;  
           D= Version number  
           R= Package Information  
 XXXXXXX: Production lot code

DIP-8	NAME Description	Description
1	CS	Current Sense pin, connect to sense the MOSFET current.
2	AC	AC/DC Brown in/out (option, can floating)
3	GND	Ground
4	FB	Voltage input pin by connecting a photo-coupler
5	VDD	Power supply pin
6,7	DRAIN	HV MOSFET Drain pin. The Drain pin is connected to the primary lead of the transformer.

**Application Circuit**



### Absolute Maximum Ratings

Parameter Symbol	Symbol	Limit Values		Unit	Remark	
		Min.	Max			
Supply Voltage VDD	V <sub>DD</sub>	-0.3	32	V		
AC,FB,CS Voltage	V <sub>AC</sub> ,V <sub>FB</sub> ,V <sub>CS</sub>	-0.3	7	V		
Drain Voltage	V <sub>D</sub>	650		V		
Max Junction Temperature	T <sub>jm</sub>	-40	150	°C		
Operation Junction Temperature	T <sub>j</sub>	-40	125	°C		
Operation Ambient Temperature	T <sub>A</sub>	-25	85	°C		
Storage Temperature	T <sub>stg</sub>	-55	150	°C		
Absolute Max. IDD Current @ V <sub>DD</sub> =25V	Ta = 25°C	I <sub>DD_max</sub>	-	22	mA	DIP-7
Power Dissipation		PD	-	1500	mW	
Junction-to-Ambient Thermal Resistance*		θ <sub>JA</sub>	-	80	°C/W	
Junction-to-Case Thermal Resistance**		θ <sub>JC</sub>	-	20	°C/W	
Lead temperature (Soldering, 10 sec)			-	260	°C	
ESD Voltage Protection	HBM	V <sub>ESD-HBM</sub>	-	3.0	KV	
	MM	V <sub>ESD-MM</sub>	-	300	V	

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
Operation Junction Temperature	T <sub>jo</sub>	-40	125	°C	
Supply Voltage V <sub>DD</sub>	V <sub>DD</sub>	11	25	V	
Startup Resistor Value	R <sub>star</sub>	1	14	MΩ	
Ambient temperature range	T <sub>opr</sub>	-25	85	°C	
Capacitance of CS pin	C <sub>CS</sub>	47	390	pF	
Capacitance of FB pin	C <sub>FB</sub>		2.2	nF	

### DC Electrical Characteristics (VCC =15V, Ta=25°C)

#### Supply Voltage (VCC Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Startup Current	I <sub>CC-ST</sub>	2	3.5	5.5	μA	UVLO ON - 0.1V
Operating Current (with 1nF load on DRV pin)	I <sub>CC-OP</sub>	0.4	0.6	0.8	mA	V <sub>FB</sub> =0V
	I <sub>CC-OP</sub>	1.5	2	2.5	mA	V <sub>FB</sub> =2.5V CL=1nF
	I <sub>CC-OLP</sub>	0.2	0.35	0.5	mA	OLP
UVLO (off)	V <sub>UVLO-OFF</sub>	7.5	8.0	8.5	V	
UVLO (on)	V <sub>UVLO-ON</sub>	16		19	V	
V <sub>DD</sub> OVP Level	V <sub>OVP</sub>	26	27	28.5	V	
OVP Debounce Time	T <sub>OVP</sub>		4		cycle	Guarantee by Design
V <sub>CC</sub> Simulation mode(ON)	V <sub>CC-HD_ON</sub>	9.7	10.2	10.7	V	
V <sub>CC</sub> Simulation mode(Off)	V <sub>CC-HD_OFF</sub>	10.2	10.7	11.2	V	
Latch off mode release Current	I <sub>DD-LHOFF</sub>			25	uA	Guarantee by Design

#### Voltage Feedback(FB Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	I <sub>zero</sub>	0.1	0.14	0.18	mA	V <sub>FB</sub> =0V
Open Loop Voltage	V <sub>FB-OP</sub>	4.8	5	5.2	V	FB pin open
Over Load Protection	V <sub>OLP</sub>	3.5	4	4.5	V	

Debounce Time of OLP	T <sub>OLP</sub>	90	100	110	ms	
Burst mode start voltage(on)	V <sub>BUR_ON</sub>	0.35	0.45	0.55	V	
Burst Mode Hysteresis	V <sub>BUR_HY</sub>	0.05	0.1	0.15	V	
Green Mode Threshold	F <sub>th_GR</sub>	35	45	55	KHz	V <sub>FB</sub> =1.3V

**Current Sensing (CS Pin):**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time & Propagation Delay to Output	T <sub>LEB +TPD</sub>	400	500	600	ns	
Maximum CS Off Voltage	V <sub>CSO</sub>	0.65	0.7	0.75	V	
OCP source current	I <sub>OCP</sub>	240	250	260	uA	Min. Duty
CS Over Voltage Protection	V <sub>CS_OVP</sub>	0.45	0.5	0.55	V	T = T <sub>off</sub>
OVP Leading Blanking time	T <sub>OVP_LEB</sub>		2		us	Guarantee by Design
Internal Slope Compensation	V <sub>SLOPE</sub>		160		mV	
Short Circuit Protection Voltage	V <sub>SCP</sub>		0.85		V	
Debounce Time of V <sub>SCP</sub>	T <sub>SCP</sub>		2		cycle	
Short Circuit Detection Time	T <sub>SCP</sub>		100		us	

**Alternating Current Detect(AC Pin):**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Brown In trigger point	V <sub>BNI</sub>	0.8	0.85	0.9	V	
Brown Out trigger point	V <sub>BNO</sub>	0.65	0.7	0.75	V	
BNO De-bounce time	T <sub>BNO</sub>	20	26.5	30	ms	

**Timer Section:**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F <sub>Burst</sub>	22		28	KHz	
PWM Mode Frequency	F <sub>PWM</sub>	61	65	69	KHz	
Voltage stability of Frequency	F <sub>PSRR</sub>	-1		+1	%	V <sub>DD</sub> = 11V~25V
Frequency Shuffling Range	F <sub>jitter</sub>	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D <sub>MAX</sub>	75	80	85	%	
Internal Soft Startup Time	T <sub>SS</sub>	10.3	13.2	16	mS	

**On chip Thermal shut down:**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
IOTP Level	V <sub>IOTP</sub>		150		°C	Guarantee by Design
Output High Level	V <sub>OOTP</sub>		120		°C	

**SDSP (Secondary diodes short protection):**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
SDSP CS pin level	V <sub>CS_SDSP</sub>		0.85		V	
De-bounce Cycle	T <sub>D_SDSP</sub> (*)		2		Cycle	Guarantee by Design

# EST.28xxDR

## Green-Mode PWM Controller (SSR)

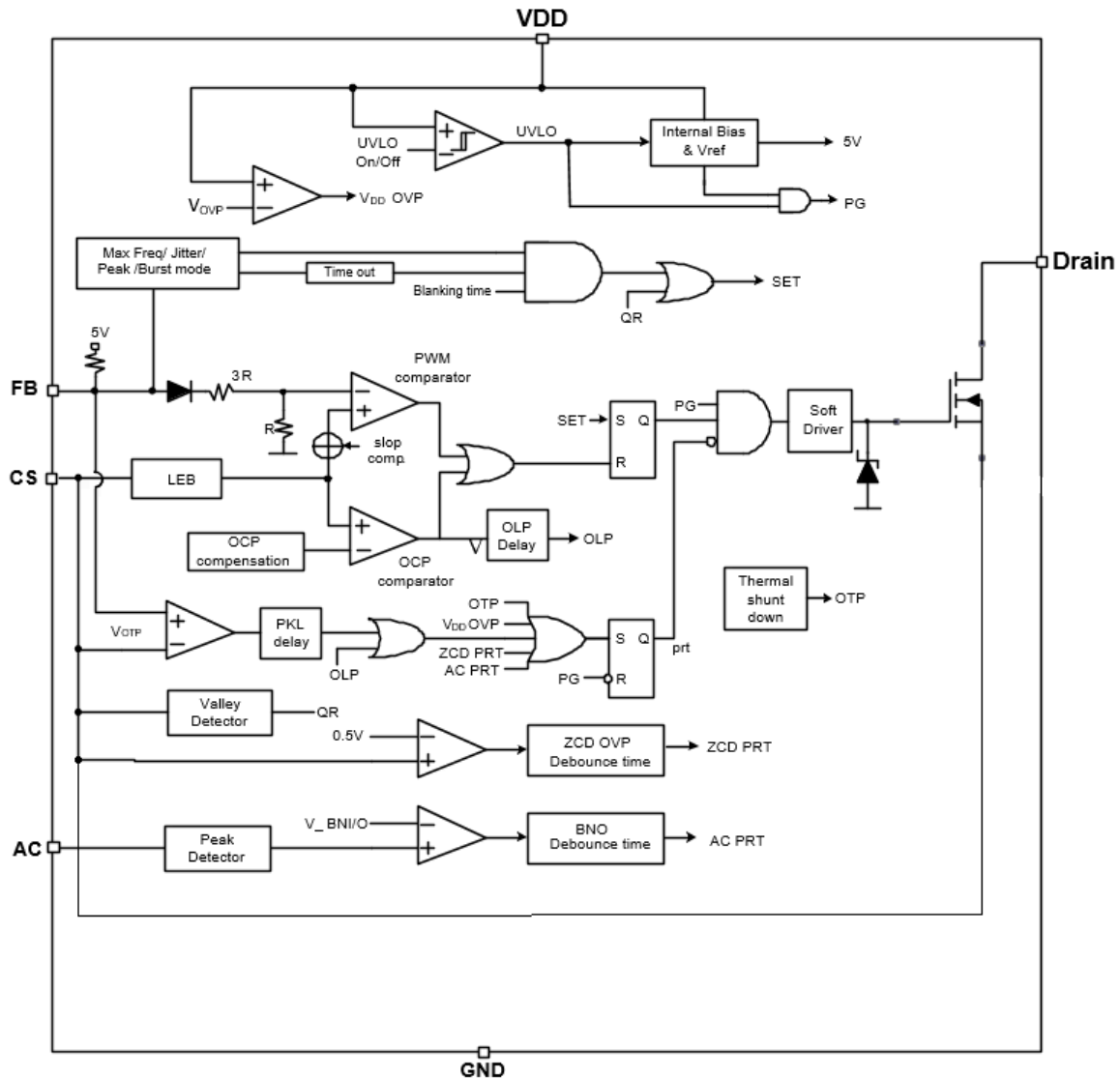


### 650V MOSFET (Drain Pin) :

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark	Package
MOSFET Drain-source Breakdown Voltage	$BV_{DSS}$	VGS=0V ID=250uA	650			V		
Static drain-source on-resistance	$R_{DS(on)}$	VGS=10V ID=0.4A		14.0	17.0	$\Omega$	EST.2810DR	DIP-8
		VGS=10V ID=0.5A		9.0	12.0	$\Omega$	EST.2812DR	DIP-8
		VGS=10V ID=1A		4.5	5.0	$\Omega$	EST.2816DR	DIP-8
		VGS=10V ID=1.5A		3.1	4.0	$\Omega$	EST.2818DR	DIP-8

### Block Diagram

#### EST.28xxDR

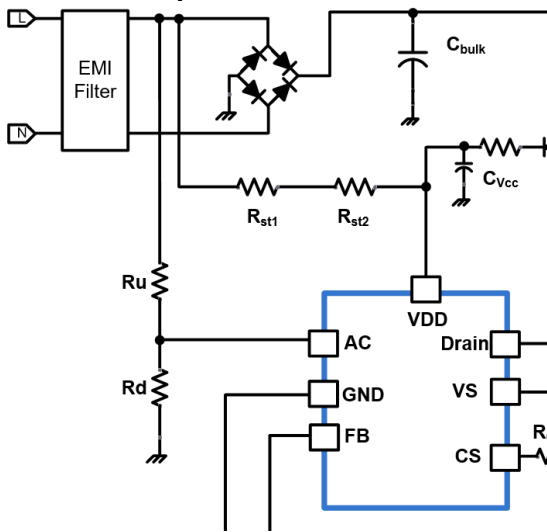


**Application Note**

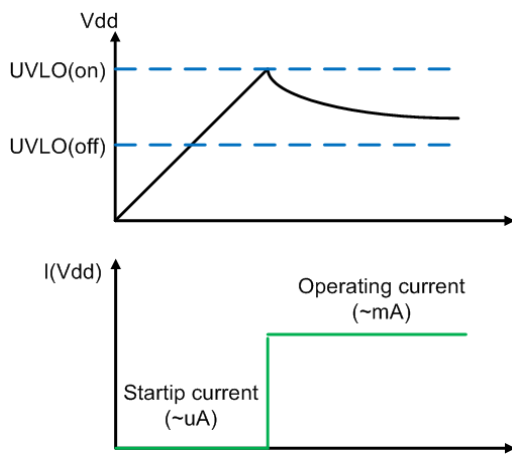
**Operation Overview**

The EST.28xxDR meets the green power requirement and very is suitable for the application for those networking adaptors and various consumer power, which can provide more power efficiency and keep lower power loss. It also supports various kind of protection for every abnormal environments.

**VDD Start-up and Control**



**Fig.1**



**Fig.2**

The start-up circuit of EST.28xxDR is shown in Fig.1 . The internal comparator of EST.28xxDR will detect the voltage on the VDD pin, and assures the supply voltage enough to turn it on. At beginning, the startup current

provides by  $(R_{st1}/R_{st2})$  to charge the capacitor  $C_{VDD}$  till VDD gets enough voltage (UVLO\_ON) to turn on

itself, please refers to Fig.2. Meantime, it goes a step further to deliver the gate drive signal to enable the Aux. winding of transformer , and then provides supply current. The startup current of EST.28xxDR is designed to be very low so that  $C_{VDD}$  could be charged up above the threshold of UVLO\_on and it starts up quickly.

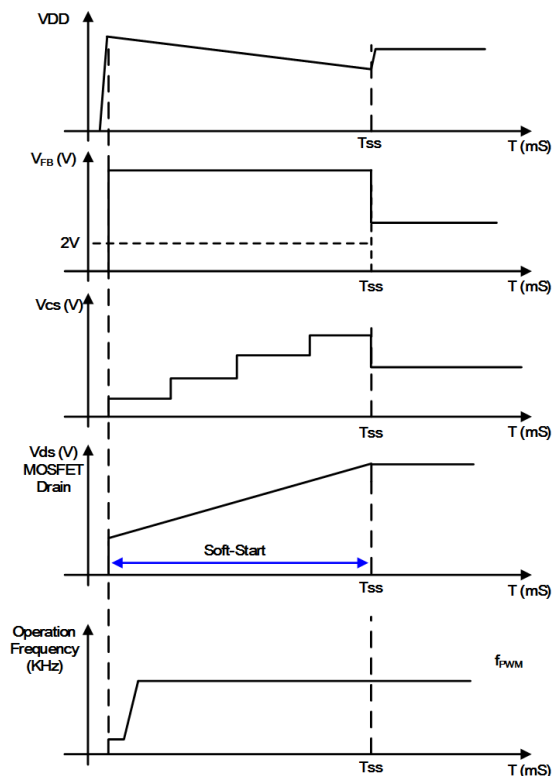
EST.28xxDR series are process with low power mix-mode process (5V and 32V), which max start-up current is below 3uA. R-start calculate as below :

$$\frac{V_{bulk} - V_{UVLO\_ON}}{R_{start}} > I_{CC - ST}$$

It is trade-off between startup time and low start-up consumption with a higher startup resistance. Therefore, carefully selects the value of  $R_{start}$  and  $C_{VDD}$  to optimize the power consumption and startup time.

**SS , Soft-start Sequence**

EST.28xxDR also builds up 13.2/8.6 ms (typical) soft-start to soften the electrical stress occurring in the power supply during startup, refer to Fig.3. As soon as VDD reaches UVLO\_on, the Cs peak voltage is gradually increased from 0.2V to the maximum level, see Fig.3.



**Fig.3**

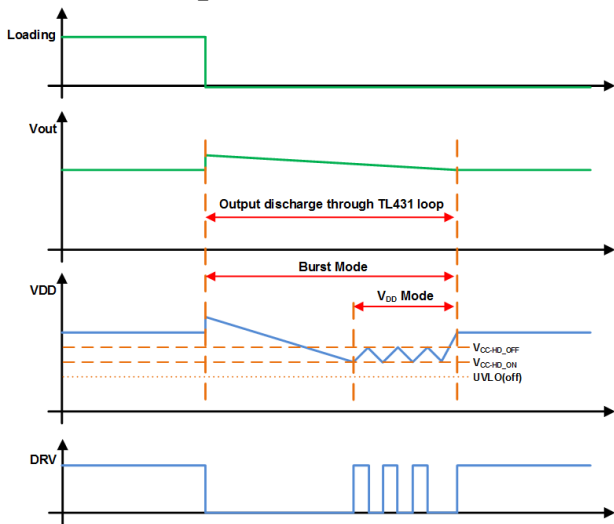
**VDD Stimulation Mode**

EST.28xxDR provides stimulation mode to avoid abnormal re-start-up under the situation of heavy loading to no-load, caused by non-balance of discharge of VDD cap and output cap, which is different with burst mode. The waveform is shown in Fig.4

Condition :  $V_{FB} < V_{BUR\_ON}$  &  $V_{DD} < 9.5V$  trigger, Hysteresis Voltage 1V

Action : IC fix output  $F_{Burst}$  , and  $V_{CS}$  keeps as 0.15V

Notice : Design  $V_{AUX}$  higher than 11V



**Fig.4**

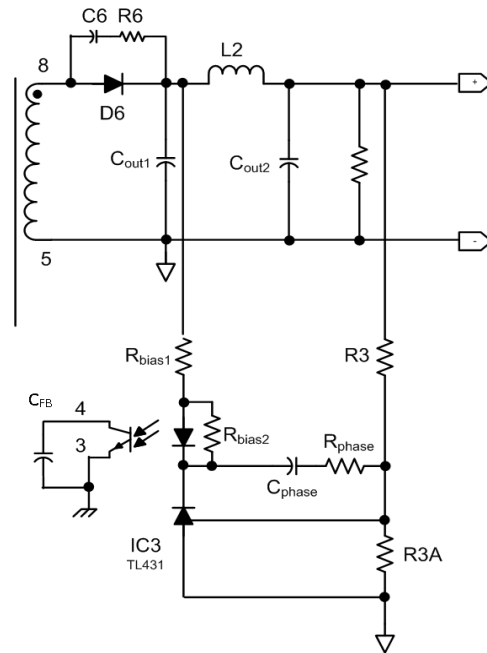
**FB , Voltage Feedback Loop**

EST.28xxDR uses current mode control, that is say, the voltage feedback signal is provided from EST.431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

- (1).  $R_{bias1}$  and  $R_{bias2}$  to prevent the abnormal output voltage at heavy loading. Generally, we suggest  $R_{bias1}$  100~1K $\Omega$ ,  $R_{bias2}$  1.5~2.5K $\Omega$
- (2).  $R_{phase}/C_{phase}$  is for RC phase compensation and prevent oscillate to adjust the value of  $C_{FB}$
- (3). Generally, we suggest  $R_{phase}$  1~10K $\Omega$  ,  $C_{phase}$  0.1 $\mu$ F ,  $C_{FB}$  1~2.2nF
- (3). The ratio of  $R_3$  and  $R_{3A}$  is depend on the output voltage spec (EST. 431 ,  $V = 2.5V$ )



**Fig.5**

In addition,  $V_{FB}$  is also used to determine the green mode level .When  $V_{FB}$  is under  $V_{BUR\_ON}$  , it is under no load or light load condition; at light loading, burst mode can effectively reduces the switching loss. When  $V_{FB}$  is larger than  $V_{BUR\_ON}$ , it will leave away the standby mode. The normal operation of  $V_{FB}$  is from  $V_{BUR\_ON}$  to 2.4V meanwhile, short-circuit current is around  $I_{Zero}$ .

**CS, Current sense Loop**

Current mode PWM control mode detects the current command (CS) from the Rsense (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continues conduction mode (CCM) , therefore, EST.28xxDR also builds in the slope compensation between high and low AC line to avoid



the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS pin being damaged by the unknow negative spike.

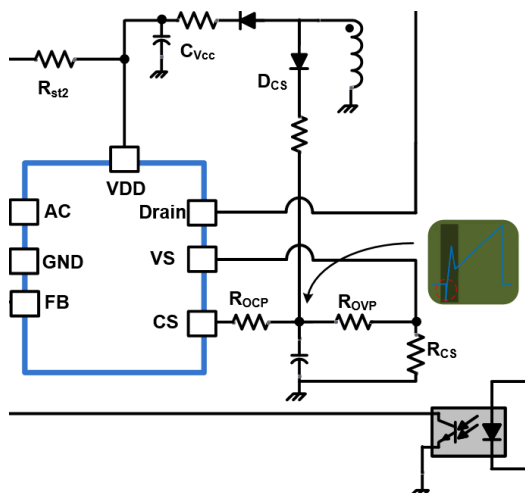


Fig.6

### Complete Protection

EST.28xxDR integrates various kind of protection to make sure operation safety.

#### VDD OVP (Over Voltage Protection)

The maximum ratings of the EST.28xxDR are around 30V.

To prevent the VDD enter breakdown condition, EST.28xxDR series are integrated with OVP function on VDD pin. Whenever the VDD voltage is higher than the  $V_{OVP}$  threshold, the output gate drive circuit will be turn-off simultaneously and the power MOSFET is turn-off until the next UVLO(on) cycle.

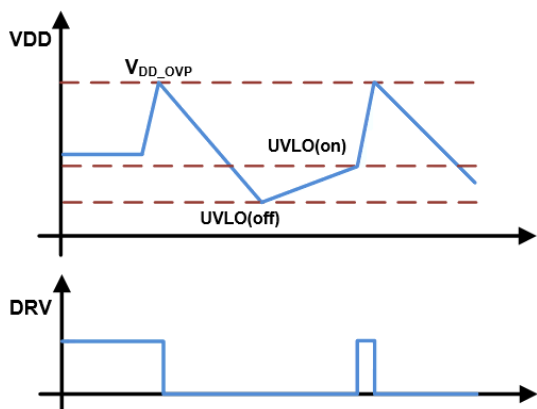


Fig.7

#### SDSP, Secondary Diode Short Protection

After short circuit of 2<sup>nd</sup> side schottky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high Vds to damage MOSFET.

EST.28xxDR detects the inductance current through the resistance, Rcs, of CS pin, and will trigger protection (latch or hiccup) when Vcs higher than 0.85V and sustains 2cycle timing.

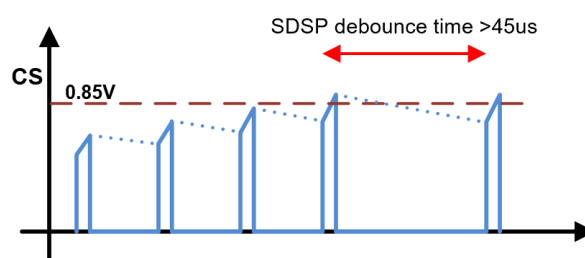


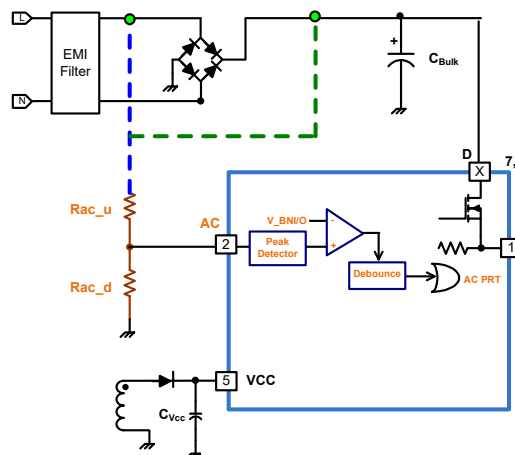
Fig.8

#### AC/DC Brown-in/out protection

This AC pin is option, and can be floating.

The EST.28xxDR has a built-in internal brown-in/out protection comparator monitoring voltage of AC pin. Fig. xx shows a resistive divider with low-pass filtering for line-voltage detection on the AC pin, which can detects before AC bridge ,DC bulk capacitance or let it float.

If the AC pin voltage is lower than 0.7V, the PWM gate is disable to protect the system over current. If the AC pin increases above 0.85V, the EST.28xxDR starts up.

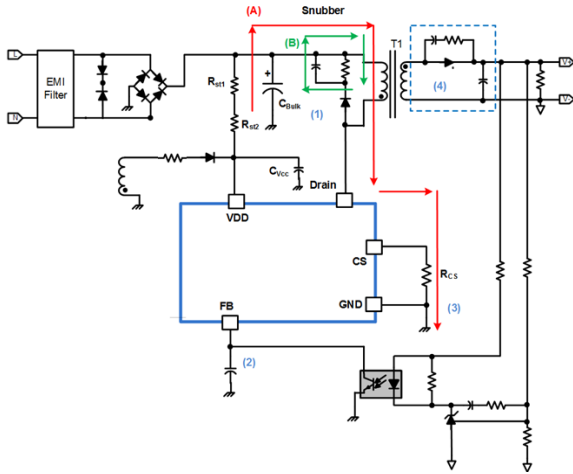


$$V_{AC} = V_{IN} \times 1.414 \times \frac{R_{ac\_u}}{R_{ac\_u} + R_{ac\_d}} > V_{BNI}$$

**Layout Guide line**

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

- ◆ **Big current path** : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area
- ◆ **Low voltage area** : R divider need to be as near FB\_Pin as possible.
- ◆ **Secondary Side Schottky** : routing as close as possible
- ◆ **Grounding** : (2) and (3) grounding separated with each other, and end connects to (1) ground.

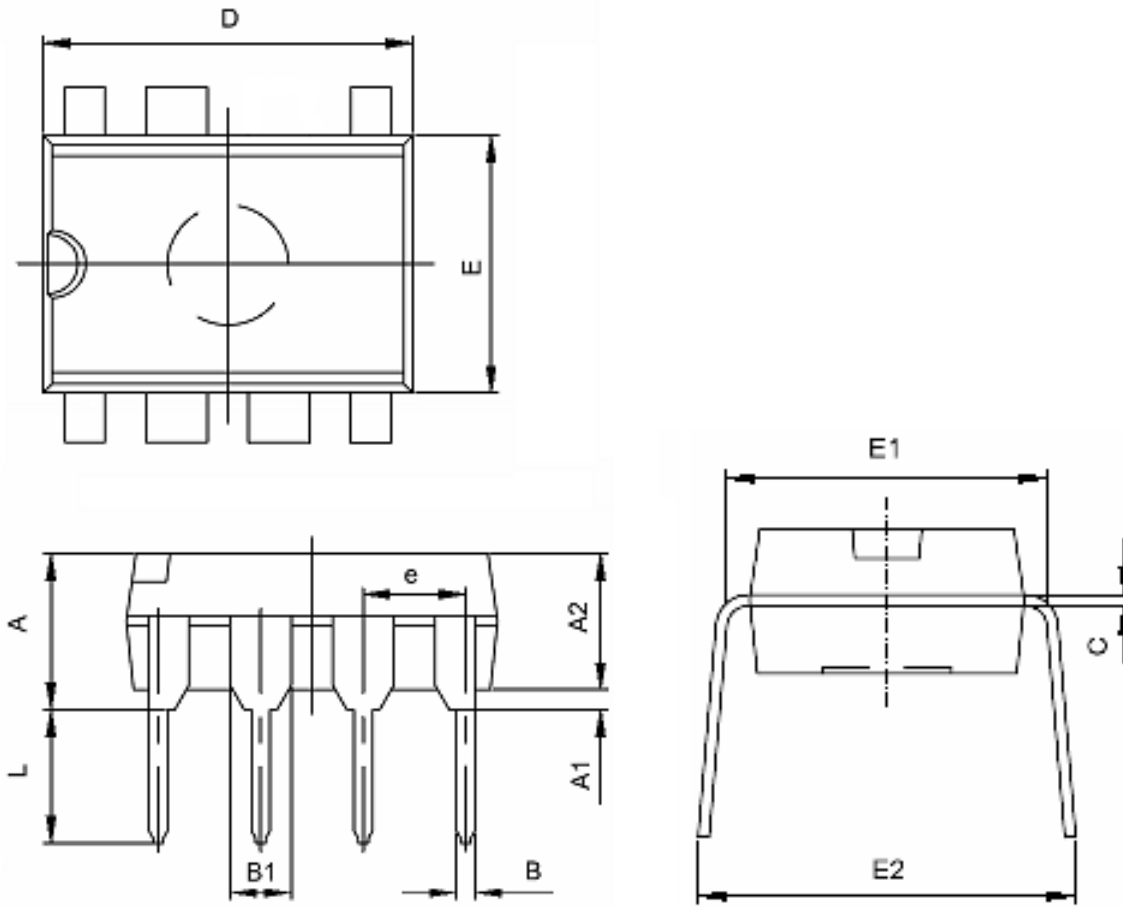


**Table 1: Complete Protection**

Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VDD OVP	VDD	VDD > 26V
1st	V-Sense	VDD UVLO Off	VDD	VDD < 7.5V
1st	V-Sense	CS pin open	CS	V <sub>CS</sub> > 0.7V after 4 cycles
2nd	SDSP	2nd side Schottky short	CS	VCS > 0.85V after 2 cycles
2nd	SCP	Output short	CS	1. 12ms blank time during start-up 2. after 4 cycles 3. Duty < 10%
2nd	OVP	Output OVP	CS	Vcs compares to 0.5V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS=0.7V
2nd	OLP	OLP	FB	CS > 4V
IC	Chip OTP			chip OTP at 150 °C

**Package Information**

DIP-7 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370



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