Data Sheet

Type Description : Multi-Mode Flyback PWM Controller

Product Name : EST.27xxA

Reversion : V1.0

Reversion Date : May, 2019

Page : 15 Pages

EST.27xxA
Multi-Mode Flyback PWM Controller

General Description

EST.27xxA series integrate a dedicated multi- mode PWM controller with a high voltage power MOSFET. It provides several functions to enhance the efficiency to meets the criteria of global standards such as DoE Level VI and EU CoC V5 Tier-2. Meantime, it also provides excellent EMI-improved solution, and also built in complete protection.

EST.27xxA is a multi-mode controller. At full load, the IC operates in fixed frequency CCM mode or QR mode based on the AC line. In this way, high efficiency in the universal input voltage at full load can achieved. At normal load, It operates in QR mode. When the load goes low, it operates in Green mode with Valley switching for high efficiency. When the load is very small, the IC operates in Burst mode to minimize the standby power loss. As a result, high efficiency can be achieved in the whole loading range.

EST.27xxA also built-in the leading-edge blanking (LEB) of the current sensing and feedback loop to screen the spike noise from any input signal. The internal slope compensation can limit the constant output over universal AC input range. The sawtooth over frequency function for EMI improved solution.

Meanwhile, EST.27xxA also provides various protection, such as, OLP (Over Load Protection) ,VDD OVP (Over Voltage Protection) , Output OLP and output OVP to prevent the circuit damage from the abnormal conditions.

EST.27xxA is available in SOP-7/DIP-7 .

EST.27xxA works with current sensing synchronous rectifier controllers, such asEST.61xxA, to achieve higher conversion efficiency and very compact power density.

Features

- 65KHz fix frequency mode at PWM Mode
- Internal 12ms Soft-start in 65KHz
- Very low startup current (<6 uA)
- 0.5mA ultra-low operating current at light load
- Programmable adaptive burst control for light-load efficiency with low output ripple and audible noise suppression.
- Programmable adaptive Frequency Shuffling and Slope Compensation @ QR and PWM Mode
- Current mode control with Cycle-by-Cycle current limit
- Built-in slope and load regulation compensation
- LEB (Leading-edge blanking) on CS Pin
- UVLO (Under voltage lockout)
- Fault Protections : VCC Over Voltage, RTL OVP(Over Voltage & UVP (Under Voltage), Output Short-Circuit, Over-Current, OLP (Over load protection) OTP(Over temperature protection) and Pin Fault
- Photo coupler short protection & Feedback open protection
- High voltage CMOS process with excellent ESD protection
- Hazardous Substance Free
- RoHs/REACH Compliant

SOP-7L

DIP-7L

Application

- Switching AC/DC adapter and battery charger
- ATX standby power
- Open frame switching power and CD(R)
- Set-top-boxes(STB) 384Xreplacement

Function and Protection Options

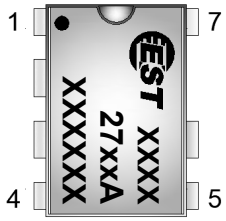
Part No.	Package	Freq.	Protection					
		KHZ	VCC OVP	OLP	AUX. OVP	AUX. UVP	CS Open	SDSP
EST.27xxA	SOP7/DIP-7	65KHz	Hiccup	Hiccup / 65mS	Hiccup	Hiccup	Hiccup	Hiccup

Note: EST lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. EST lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. EST defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

Ordering Information

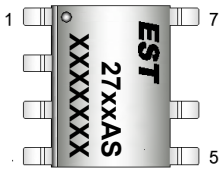
Part Number	Package	Packaging	Note
EST27xxAS	SOP-7L	Tape & Reel	Green
EST27xxA	DIP-7L	Tape	Green

Pin Assignments and Package Type



DIP-7

EST: LOGO
XXXX: Dote Code
27xxA: xx=MOS Type;
XXXXXX: Production lot code

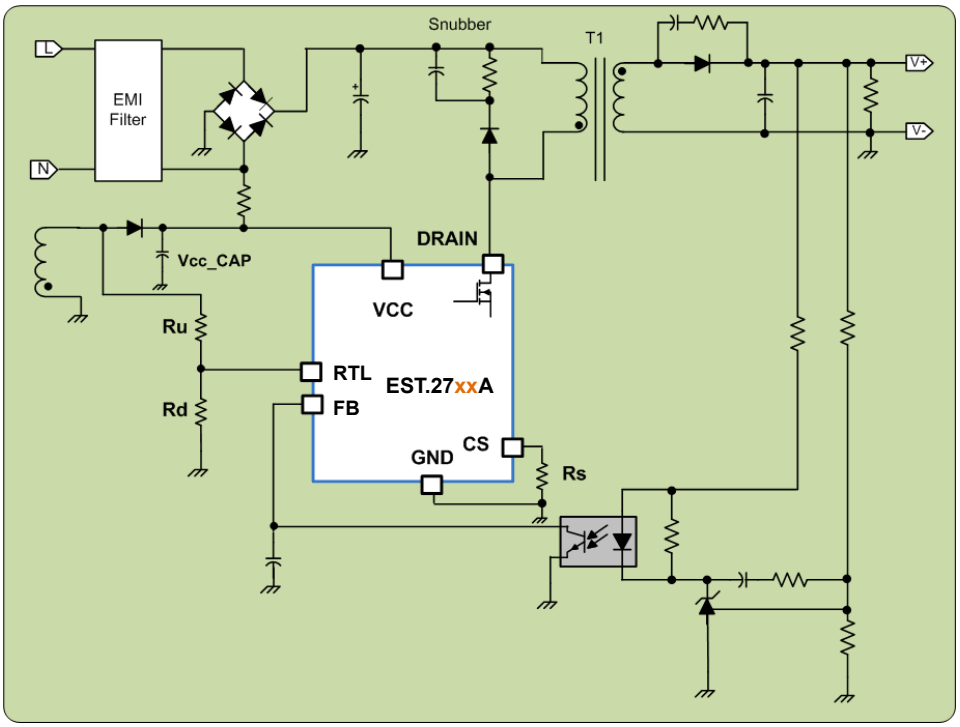


SOP-7

EST: LOGO
27xxAS: xx=MOS Type;
S= Smd
XXXXXXX: Production lot code

DIP/SOP-7	NAME Description	Description
1	VCC	Power supply pin
2	FB	Voltage input pin by connecting a photo-coupler
3	RTL	Multiple functions. Auxiliary voltage sense, Quasi Resonant and Vout OVP&UVP detection.
4	CS	Current Sense input. The current sense resistor between this pin and GND is used for current limit setting.
5,6	DRAIN	HV MOSFET Drain pin. The Drain pin is connected to the primary lead of the transformer.
7	GND	Ground

Application Circuit



Absolute Maximum Ratings

Parameter Symbol		Symbol	Limit Values		Unit	Remark
			Min.	Max		
Supply Voltage VDD		V_{DD}	-0.3	32	V	
AC,FB,CS,RTL Voltage		V_{AC},V_{FB},V_{CS},V_{RTL}	-0.3	7	V	
Gate Driver Voltage		V_{GATE}	-0.3	V_{DD}+0.3	V	
Maximum Junction Temperature		Tj		150	℃	
Operation Ambient Temperature		TA	-25	85	℃	
Storage Temperature		T_{stg}	-55	150	℃	
Power Dissipation	Ta = 25℃	PD	-	1.1	W	DIP-7(1)
Junction-to-Case Thermal Resistance**		θ_{JC}		20	℃/W	
Junction-to-Top Thermal Resistance***		θ_{JT}		35	℃/W	
Junction-to-Ambient Thermal Resistance*		θ_{JA}		150	℃/W	SOP-7L
Junction-to-Case Thermal Resistance**		θ_{JC}		39	℃/W	
Lead temperature (Soldering, 10 sec)			-	260	℃	
ESD Voltage Protection	HBM	$V_{ESD-HBM}$	-	3.0	KV	
	MM	V_{ESD-MM}	-	300	V	

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.
*Free standing with no heatsink; withoud copper clad.(Measurement condition – just before junction temperature TJ enters into OTP)
**Measure on the DRAIN pin close to plastic interface
***Measure on the PKG top surface

Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
Operation Junction Temperature	Tjo	-40	125	℃	
Supply Voltage V_{DD}	V_{DD}	10	25	V	
Startup Resistor Value	R_{star}	1	14	MΩ	
Ambient temperature range	T_{opr}	-40	85	℃	
Capacitance of FB pin	C_{FB}		2.2	nF	

DC Electrical Characteristics (VCC =15V, Ta=25°C)

Supply Voltage (VCC Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Startup Current	I_{CC-ST}	2	3.5	5.5	μA	UVLO ON - 0.1V
Operating Current (with 1nF load on DRV pin)	I_{CC-OP}	0.4	0.6	0.8	mA	V_{FB}=0V
	I_{CC-OP}	1.5	2	2.5	mA	V_{FB}=2.5V CL=1nF
	I_{CC-OLP}	0.2	0.35	0.5	mA	OLP
UVLO (off)	$V_{UVLO-OFF}$	7.5	8.0	8.5	V	
UVLO (on)	$V_{UVLO-ON}$	17	18	19	V	
V_{DD} OVP Level	V_{OVP}	26	27	28	V	
OVP Debounce Time	T_{OVP}		4		cycle	Guarantee by Design
V_{CC} Simulation mode(ON)	V_{CC-HD_ON}	9.7	10.2	10.7	V	
V_{CC} Simulation mode(Off)	V_{CC-HD_OFF}	10.2	10.7	11.2	V	

Voltage Feedback(FB Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	I_{Zero}	0.10	0.14	0.18	mA	V_{FB}=0V
Open Loop Voltage	V_{FB-OP}	4.8	5.0	5.2	V	FB pin open
Burst mode start voltage(on)	V_{BUR_ON}	0.9	1.0	1.1	V	
Burst Mode Hysterics	V_{BUR_HY}	0.05	0.1	0.15	V	
Green Mode Threshold	V_{th_GR}		45		KHz	FB=1.3V

Current Sensing (CS Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time	T_{LEB}	300	400	500	ns	
Propagation Delay to Output	T_{pd}	300	400	500	nS	
Maximum CS Off Voltage	V_{CSTH1}	0.65	0.70	0.75	V	
OCP source current	I_{OCP}	18.5		21.5	%	I_{OCP}/I_{AUX}
Over Load Protection	V_{OLP}	0.45	0.50	0.55	V	T_{ON}
Debounce Time of OLP	T_{OLP}	54	64	74	mS	
Over temperature protection	V_{OTP}	0.45	0.5	0.55	V	T_{OFF}
Debounce Time of OTP	T_{OTP}	54	64	74	mS	
Short Circuit Detection Time	T_{SCP}		100		uS	T_{ON}
Short Circuit Protection Voltage	V_{SCP}		0.85		V	
Debounce Time of VSCP	T_{SCP}		2		cycle	

Multiple functions. Auxiliary voltage sense (ZCD Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output OVP Trigger Point	V_{TH_OVP}	2.9	3.0	3.1	V	FB>4
Output OVP Deglitch Time Constant	$T_{\_OVP\_delay}$		4.0		Cycle	Guarantee by Design
Output UVP Trigger Point	V_{TH_OVP}	0.7	0.8	0.9	V	FB>4
Output UVP Deglitch Time Constant	$T_{\_OVP\_delay}$		4.0		Cycle	Guarantee by Design
Positive Clamped voltage	V_{POS}	6.0		7.0	V	
Negative Clamped voltage	V_{NEG}	-0.05		0.05	V	
RTL Leading Blanking time	T_{RTL_LEB}		2.0		uS	Guarantee by Design
QR Detection Time	T_{QR}		3.0		uS	

Timer Section:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F_{Burst}	20	22.5	25	KHz	
PWM Mode Frequency	F_{PWM}	61	65	69	KHz	
Voltage stability of Frequency	F_{PSRR}	-1		+1	%	V_{DD} = 11V~25V
Frequency Shuffling Range	F_jitter	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D_{MAX}	70	75	80	%	
Internal Soft Startup Time	T_{SS}	10		15	mS	

On chip Thermal shut down:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
IOTP Level	V_{IOTP}		150		℃	Guarantee by Design
Output High Level	V_{OOTP}		120		℃	

650V MOSFET (Drain Pin) :

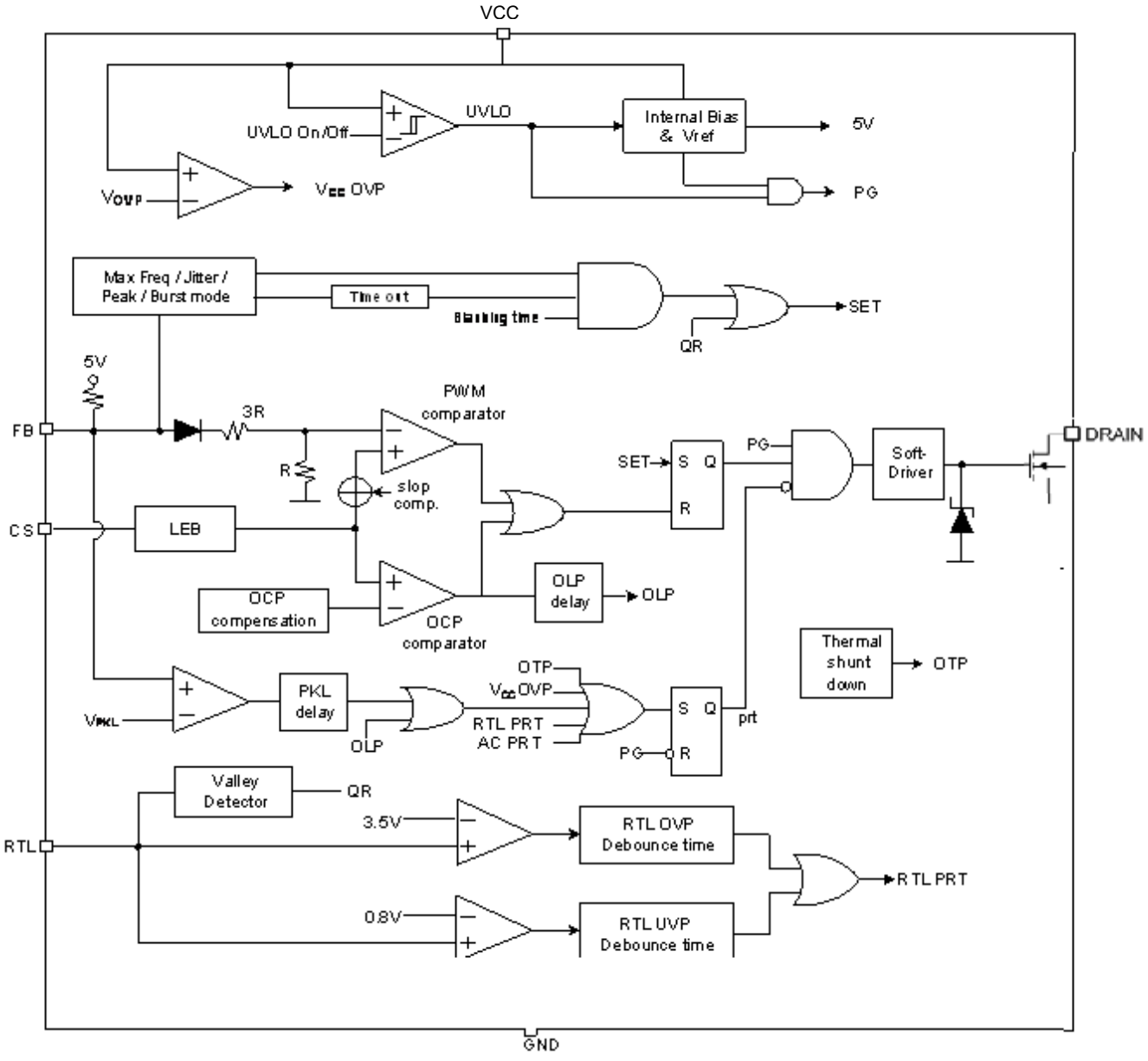
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark	Package
MOSFET Drain-source Breakdown Voltage	BV_{DSS}	VGS=0V ID=250uA	650			V		
Static drain-source on-resistance	$R65_{(on)}$	VGS=10V ID=0.4A		14	17	Ω	EST.2708AS	SOP-7
							EST.2710A	DIP-7
		VGS=10V ID=0.5A		9	12	Ω	EST.2710AS	SOP-7
							EST.2712A	DIP-7
		VGS=10V ID=1A		4.5	5	Ω	EST.2712AS	SOP-7
							EST.2716A	DIP-7
		VGS=10V ID=1.5A		3.1	3.9	Ω	EST.2716AS	SOP-7
							EST.2718A	DIP-7
		VGS=10V ID=2.0A		2.2	2.6	Ω	EST.2720A	DIP-7

700V MOSFET (Drain Pin) :

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark	Package
MOSFET Drain-source Breakdown Voltage	BV_{DSS}	VGS=0V ID=250uA	700			V		
Static drain-source on-resistance	$R70_{(on)}$	VGS=10V ID=1.0A		2.2	2.4	Ω	EST.2718AS	SOP-7
							EST.2722A	DIP-7
		VGS=10V ID=1.0A		1.4	1.6	Ω	EST.2720AS	SOP-7
							EST.2726A	DIP-7
		VGS=10V ID=1.2A		1.0	1.1	Ω	EST.2722AS	SOP-7
							EST.2728A	DIP-7

Block Diagram

EST27xxA



Application Note

Operation Overview

The EST.27xxA meets the green power requirement and very suitable for the use in those networking adaptors ,TV open frame and various consumer power, which can provide more power efficiency and lower power loss. It also supports various kind of protection for every abnormal environments.

V_{DD} Start-up and Control

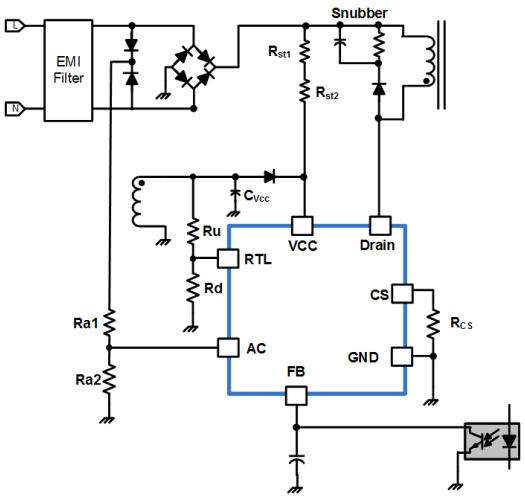


Fig-1.

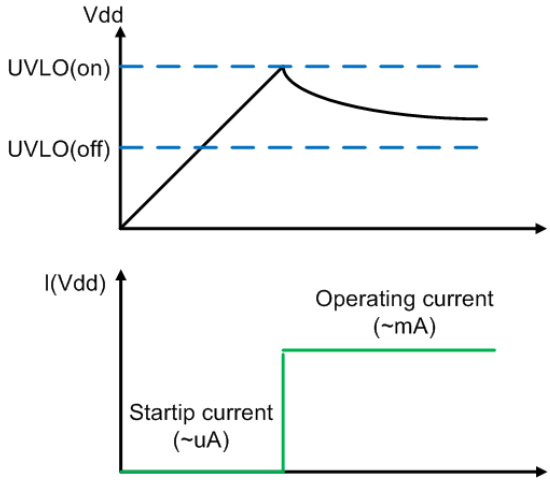


Fig-2.

The start-up circuit of EST.27xxA is shown in Fig.1 . It's internal comparator will detect the voltage on the Vcc pin, and assures the supply voltage enough to turn on the EST.27aaA. At beginning, the startup current is provided by (R_{st1}/R_{st2}) to charge the capacitor C_{VCC} till V_{CC} get enough voltage (UVLO_ON) to turn on itself, refers to fig.2. Meantime, it go a step further to deliver the gate drive signal to enable the Aux. winding of transformer , and then provides supply current. The startup current of EST.27xxA is designed to be very low so that C_{VCC} could be charged up above UVLO_on threshold level and it starts up quickly.

EST.27xxA series is process with low power mix-mode process (5V and 32V), which max start-up current is below 5.5uA。R-start calculate as below :

$$\frac{V_{bulk} - V_{UVLO\_ON}}{R_{start}} > I_{CC-ST}$$

It is trade-off between startup time and a higher startup resistance. Therefore, carefully select the value of Rstart, C_{Vcc} to optimize the power consumption and startup time.

SS，Soft-start Sequence

EST.27xxA also built-up 12.5ms (typical) soft-start to soften the electrical stress occurring in the power supply during startup, refer to Fig.3. As soon as V_{CC} reaches U_{VLO}_on, the Cs peak voltage is gradually increased from 0.2V to the maximum level, see fig.4.

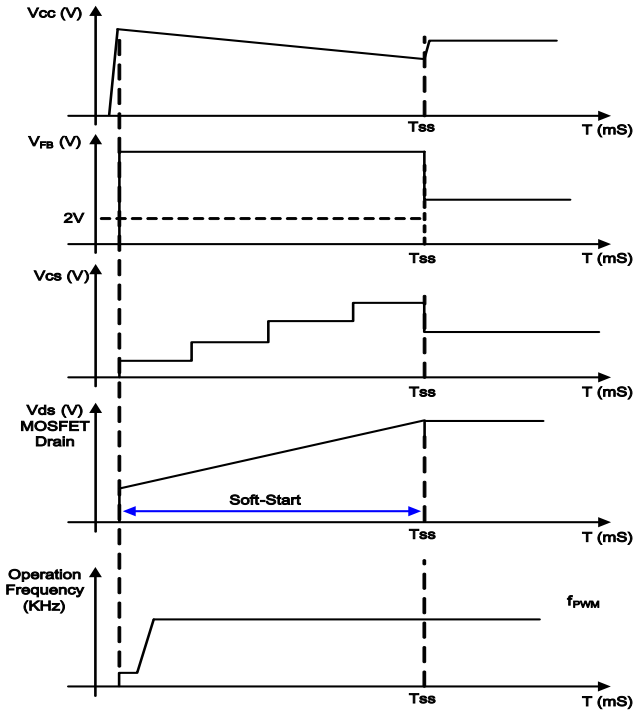


Fig.3

VDD Stimulation Mode

EST.27xxA provides stimulation mode to avoid abnormal re-start-up under heavy loading to no-load, caused by non-balance of discharge of V_{CC} cap and output cap, which is different with burst mode. The waveform is shown in fig.5.

Condition：V_{FB} < V_{BUR_ON} & $_{VCC}$ <9.5V trigger, Hysterics Voltage 1V

Action：IC fix output F_{Burst} , and V_{CS} keeps as 0.15V

Notice： Design $V_{\_AUX}$ higher than 11V

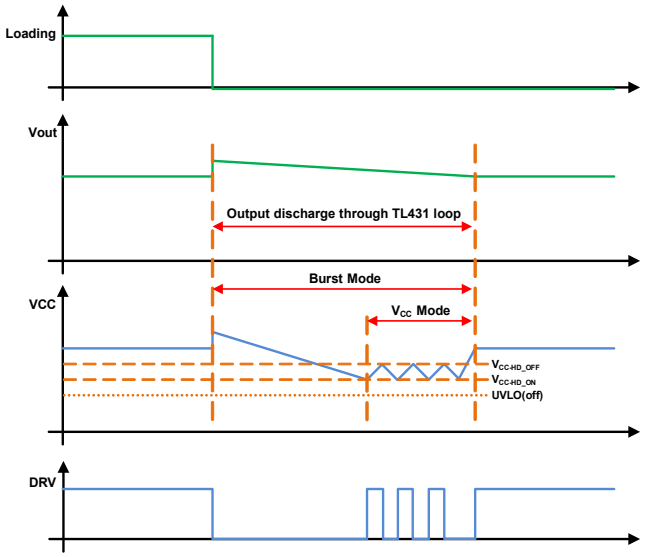


Fig.4

OLP (Over Load Protection)

EST.27xxA has new OLP built-in at CS pin, and its merit of close loop methodology makes audio noise free.

The adjustment of OCP is through RTL and CS, please refer to Fig.5. It detects the status of AC line and output voltage through the resistance divider (Ru,Rd) by the reflection waveform of Aux-winding. At negative cycle, VRTL will keep “0” and output IOCP at CS pin to change the level of slope compensation, please see Fig.5.Therefore, it can modify the Ru and ROCP to get target of OCP @full range. Please follow the procedure as below :

Step 1. Sett RU=200KΩ , Rd=39KΩ (initial setting) & ROCP = 1KΩ and modifies RCS to target of OCP@90Vac

Step 2. Increase ROCP impedance to reduce OCP and check the OCP of AC full range. Modifies ROCP to make sure the consistency of OCP for AC full ange.

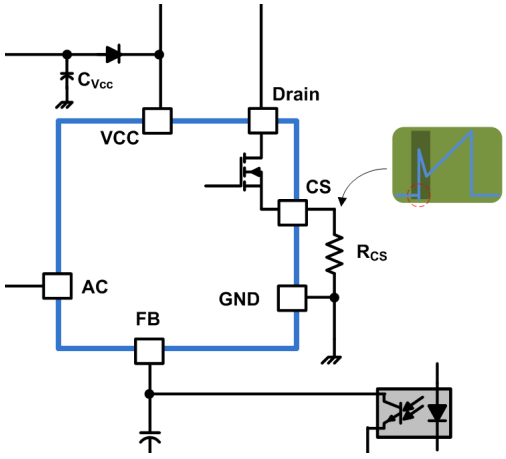


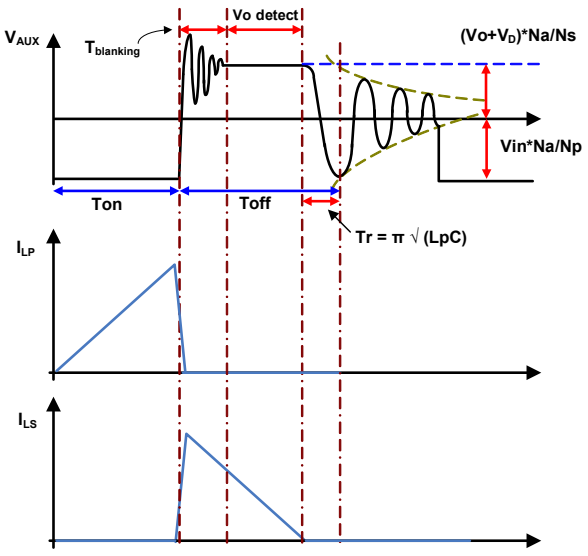
Fig.5

RTL: Demagnetization Detection from RTL pin (QR Mode Detection)

After MOSFET turns off, the current of secondary side diodes goes down to zero , and then the transformer core will be demagnetized completely, see fig.6. At the same time, a Quasi resonant signal will be detected from auxiliary winding by ZCD pin through the external resister divider.

Programmable V_{O_OVP} & burst mode level

This ZCD pin is also used to program the burst level at light load and high output voltage at system open loop . A resistive divider between Aux winding and GND is used to set a voltage at this pin to determine the peak current level when power entries the adaptive burst mode. At the same time, it also detects voltage level of output.



VO_OVP :

Modifies Rd to target of VO_OVP

Calculate the ratio of Rd to (Ru+Rd)

R_U=200Komh

$$\frac{R_d}{R_u + R_d} = \frac{V_{TH\_OVP}}{(V_{O\_OVP} + V_d)} \times \frac{N_s}{N_a}$$

Adjust Burst :

$$V_{BUR\_ON} = (V_O + V_d) \times \frac{N_a}{N_s} \times \frac{R_d}{R_u + R_d} - 1.7$$

FB，Voltage Feedback Loop

EST.27xxA series adopt current mode control, that is say, the voltage feedback signal is provided from TL431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to Considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

(1). R_{bias1} and R_{bias2} to prevent the abnormal output voltage at heavy loading. Generally, we suggest Rbias1 100~1KΩ，R_{bias2} 1.5~2.5KΩ

(2). R_{phase}/C_{phase} is for RC phase compensation and prevent oscillate to adjust the value of CFB

(3). Generally, we suggest R_{phase} 1~10KΩ，C_{phase} 0.1uF ，CFB 1~2.2nF

(3). The ratio of R_3 and R3A is Depent on the output voltage spec (TL431 ,V= 2.5V)

Fig.6

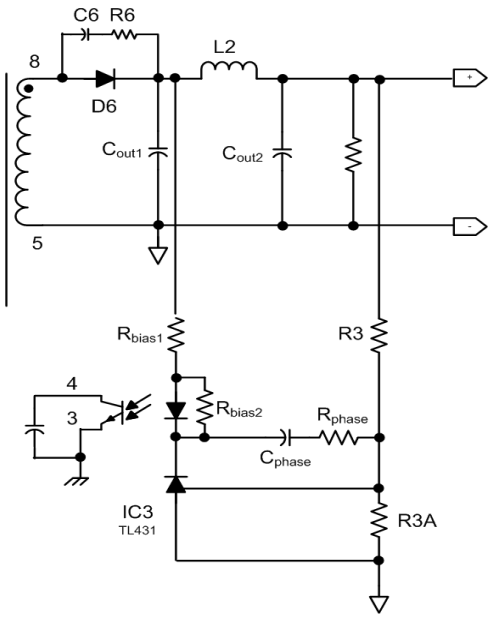


Fig.7

In addition, V_{FB} is also used to determine the green mode level .When V_{FB} is under V_{BUR_ON} , it is under no load or light load condition; at light loading, burst mode can effectively reduces the switching loss. When V_{FB} is larger than V_{BUR_ON}, it will leave away the standby mode. The normal operation of V_{FB} is from V_{BUR_ON} to 2.4V,; meanwhile, short-circuit current is around I_{Zero}.

CS, Current sense Loop

Current mode PWM control mode detects the current command (CS) from the Rsense (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continues conduction mode (CCM) , therefore, IN2P083X series of built-in high and low slope compensation to avoid the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS pin being damaged by the unknow negative spike.

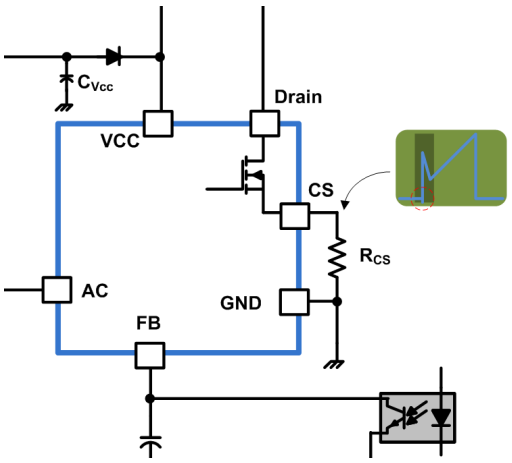


Fig.8

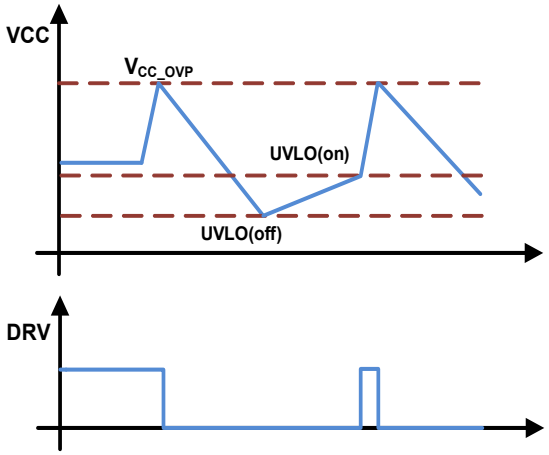


Fig.9

DRV

The driving capability of EST.2700X is around 450mA, which can support power rate around 60~70W, and it is limited the maximum duty-cycle below 80% to avoid the transformer saturation.

Typically, the threshold of MOSFET is about 20V, and the maximum clamp voltage of EST.2700X is 14V to prevent breakdown of MOSFET.

Complete Protection

EST.27xxA integrates various kind of protection to make sure operation safety.

VDD OVP (Over Voltage Protection)

The maximum ratings of the EST.27xxA are around 30V. To prevent the V_{CC} enter breakdown condition, EST.2700X series are integrated with OVP function on V_{CC} pin. Whenever the V_{CC} voltage is higher than the V_{OVP} threshold, the output gate drive circuit will be turn-off simultaneously and the power MOSFET is turn-off until the next UVLO(on) cycle.

SCP (Short Circuit Protection)

A resistive divider between Aux winding and GND is used to monitor output voltage. When output circuit is short, Therefore, as V_{RTL} is lower than 0.8V during date off region, then V_{TH_UVP} is triggered,EST.27xxA is to enable UVP function in order to reduce input power

SDSP, Secondary Diode Short Protection

After short circuit of 2nd side schotkky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high Vds to damage MOSFET.

EST.27xxA detects the inductance current through the resistance, Rcs, of CS pin, and will trigger protection (latch or hiccup) when Vcs higher than 0.85V and sustains 2cycle timing.

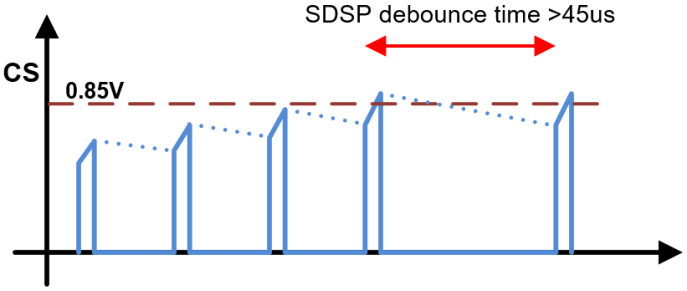


Fig.10

Layout Guide line

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

- ✓ **Big current path** : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area
- ✓ **Low voltage area :** R devider need to be as near FB_Pin as possible.
- ✓ **Secondary Side Schottky :** routing as close as possible
- ✓ **Grounding :** (2).(3) and (4) grounding separated with each other, and end connects to (1) ground.
- ✓ **RTL :** Ru & Rd as close as possible to avoid noise coupling to trigger OVP.

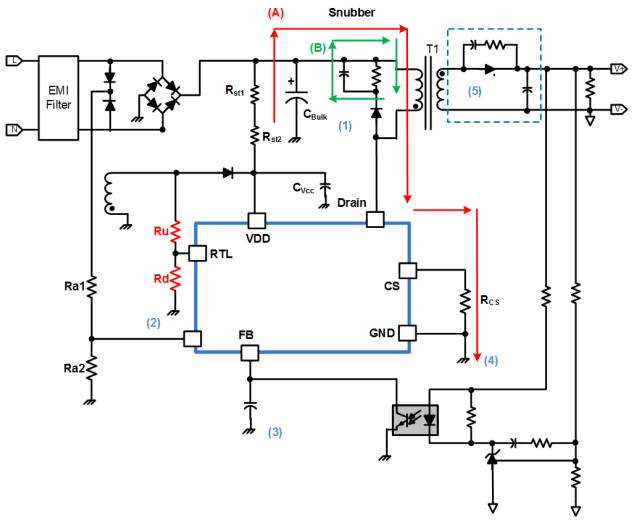
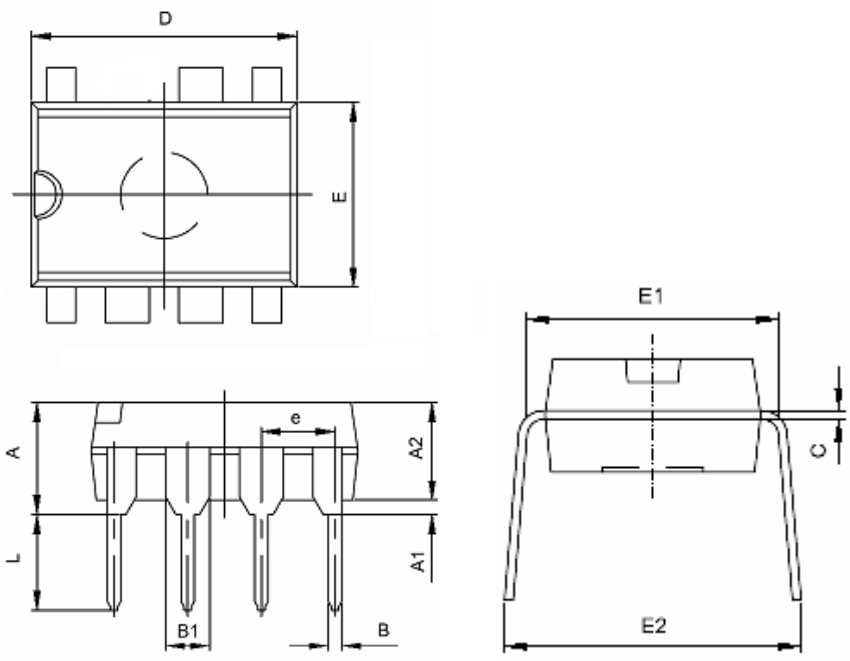


Fig.12

Table 1: Complete Protection

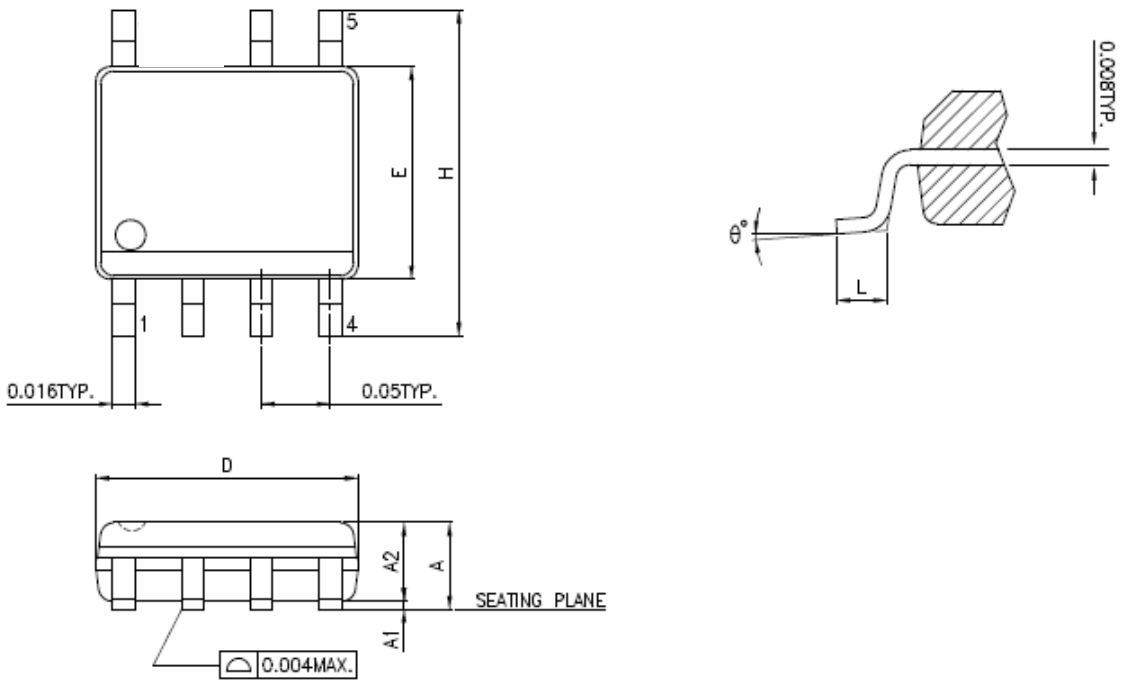
Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VCC OVP	Vcc	Vcc > 28V
1st	V-Sense	VCC UVLO Off	Vcc	Vcc < 7.5V
1st	V-Sense	Brown In Fail	AC	V_{AC}<0.85
1st	V-Sense	Brown out	AC	V_{AC}>0.75V
1st	V-Sense	Line OVP	AC	V_{AC}>3.0V
1st	V-Sense	T1 Aux gnd open	ZCD	ZCD UVP trigger
1st	V-Sense	MOS short/Gate to GND	ZCD	ZCD UVP trigger
1st	V-Sense	CS pin open	CS	V_{CS} >0.7V after 4 cycles
1st	ZCD	ZCD upper R open	ZCD	ZCD UVP : after soft-start ZCD<0.85V & FB>4V
1st	ZCD	ZCD upper R short	ZCD	ZCD OVP : ZCD>3V & FB>4V
1st	ZCD	ZCD down side open	ZCD	ZCD OVP : ZCD>3V & FB>4V
1st	ZCD	ZCD down-side short	ZCD	ZCD UVP : after soft-start time ZCD<0.85V & FB>4V
2nd	SDSP	2nd side Schottkey short	CS	VCS >0.85V after 4 cycles
2nd	SCP	Output short	ZCD	1. 12ms blank time during start-up 2. after 4 cycles 3. ZCD UVP = 0.8V & FB>4V trigger
2nd	OVP	Output OVP	ZCD	V_{ZCD} compares to 3V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS=0.7V
2nd	OLP	OLP	CS	CS > 0.5V
2nd	Short before power on		ZCD	1. 12ms blank time at start-up 2. after 4 cycles 3. ZCD UVP = 0.8V & FB>4V trigger
2nd	Short after power on		ZCD	1. after 4 cycles 2. ZCD UVP = 0.8V & FB>4V trigger
IC	Chip OTP			chip OTP at 150 ℃

DIP-7 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

SOP-7 Package (mm)



Symbols	Dimensions In Inches			Dimensions In millimeters		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	0.050	0.061	0.072	1.270	1.549	1.829
A1	0.000	------	0.010	0.000	------	0.254
A2	------	------	0.062	------	------	1.575
D	0.185	0.193	0.200	4.699	4.902	5.080
E	0.147	0.154	0.160	3.734	3.912	4.064
H	0.225	0.237	0.249	5.715	6.020	6.325
L	0.013	0.033	0.053	0.330	0.838	1.346
θ	0°	4°	8°	0°	4°	8°