DESCRIPTION

EST.2269 is highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 80W range.

PWM switching frequency at normal operation is externally programmable to tight range. At no load or light load condition, the IC operates in extended'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency in thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with EST2269. A large value resistor could thus be used in the startup circuit to minimize the standby power.

EST.2269 offers complete protection coverage with automatic self- recovery feature including Cycle-by-Cycle current limiting (OCP), over temperature protection(OTP),VDD over voltage clamp and under voltage lockout (UVLO). The Gate output is clamped to maximum 18V to protect the power MOSFET.

EST.2269 is offered in SOP-8 and DIP-8packages.

FEATURES

- Proprietary frequency shuffling technology for improved EMI performance.
- External programmable PWM switching frequency.
- Leading edge Blanking on current sense input.
- Internal synchronized slope compensation .
- Extended burst mode control for improved efficiency and minimum standby power design
- Low VDD startup current and low operating current.
- Gate output maximum voltage clamp 18V.
- Cycle-by-Cycle Current Limiting, Built-in Adaptive Current Peak Regulation
- Power on Soft-start, Programmable CV and CC Regulation
- VDD Under Voltage Lockout with Hysteresis(UVLO),OVP,OCP,OLP, ClampVDD.
- Builded-in OTP(120°C, design quaranteed.)

Applications	Ordering Information	
Offline AC/DC flyback converter for	Part number	Package
■ Battery Charger ■ Power Adaptor	EST.2269S	SOP-8
■ Set-Top Box Power Supplies ■ Open-frame SMPS	EST.2269D	DIP-8

Pin Assignments

PD8&SOP8 Package (P-DIP8&SOP8)

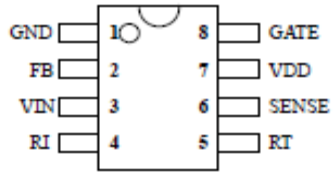


Figure 1. Pin Assignment of EST2269 for P-DIP8&SOP8

Typical Application Circuit

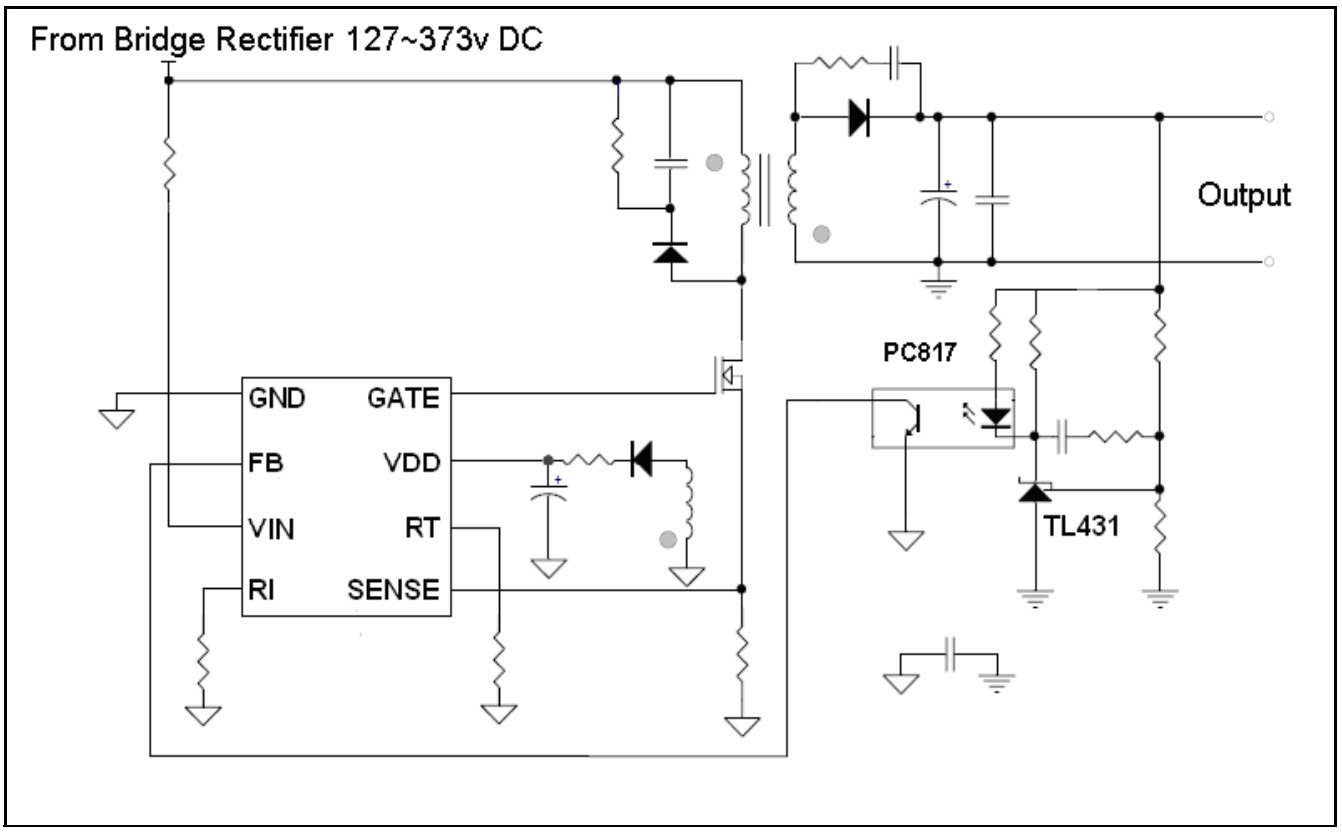


Figure2. Typical Application Circuit of EST.2269

Functional Pin Description

Pin Number	Symbol	Pin Function
1	GND	Ground
2	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin sense.
3	VIN	Star up supply and line sense Pin
4	RI	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	OTP sense pin, connect a NTC resistor to GND.
6	SENSE	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	Chip DC power supply pin.
8	GATE	Totem-pole gate drive output for the power MOSFET.

Block Diagram

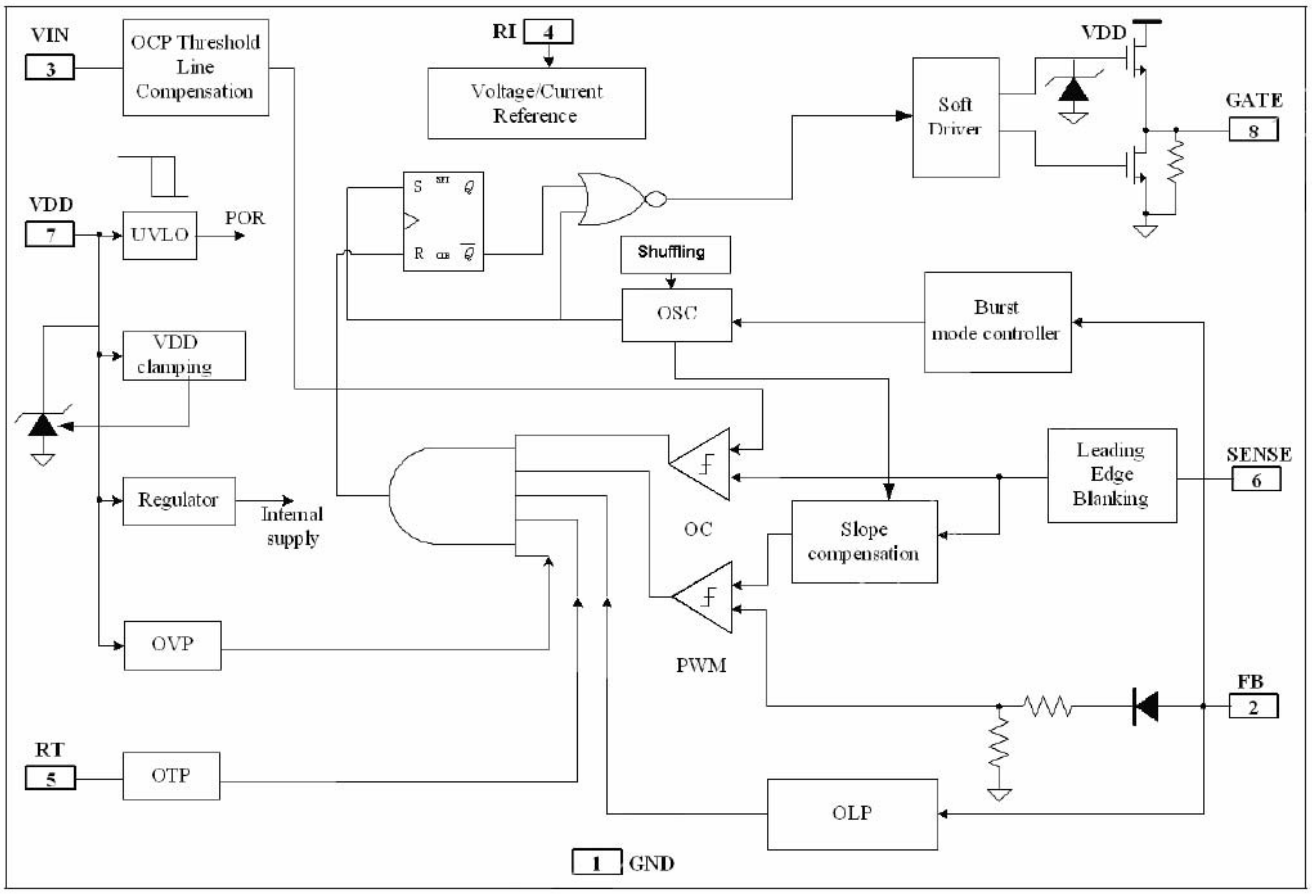


Figure 3. Block Diagram of EST.2269

Absolute Maximum Ratings

■ VDD/VIN to GND	+ 30V
■ VDD zener clamp voltage	VDDclamp+0.1 KΩ
■ VDD clamped current	10mA
■ VFB, VSENSE ,VRT and VRI to GND	- 0.3V to + 7V
■ Junction Temperature	- 20°C to + 150°C
■ Storage Temperature Range	- 55°C to + 160°C

Note：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

■ Supply Voltage, VDD	11V to + 29V
■ RI resistor value	24K-31Kohm
■ Operation Temperature Range	- 20°C to + 85°C

ESD In formations

■ Human Body Mode---------- 3000V
■ Machine Mode---------- 250V

Electrical Characteristics

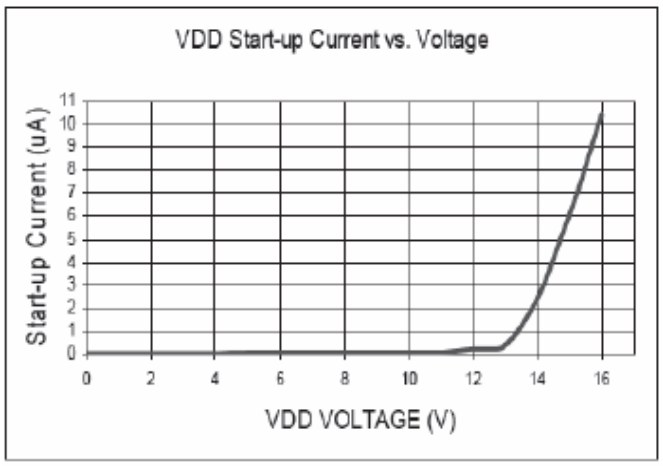
(TA = 25°C, RI=24kOhm, VDD=16V if not otherwise noted)

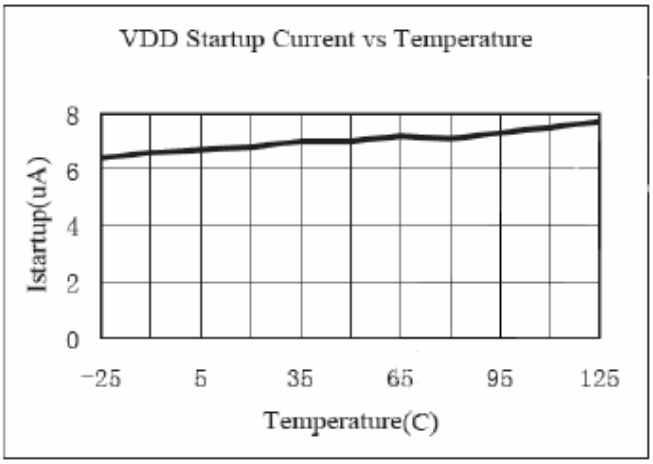
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SUPPLY SECTION						
Chip start up current via VDD pin	I_set	Vdd=15V, measure current into VDD pin		6	10	uA
Operation current	I_op	VDD=16V,VFB=3V		2.3		mA
VDD UVLO enter	U_{VLO_L}		9.5	10.5	11.5	V
VDD UVLO exit	U_{VLO_H}		15.5	16.5	17.5	V
VDD clamp voltage	V_{DD_CLP}	I(VDD)=10mA	29	30	31	V
OVP enter	O_{VP_ON}		24	26.5	27.5	V
OVP hysteresis	O_{VP_Hys}	OVP_ON-OVP_OFF		2		V
OVP debounce time	T_{D_OVP}			80		uS
FEEDBACK SECTION						
PWM input gain	$A_{\_PWM}$	ΔVFB/ΔVCS		2.8		V
VFB open loop voltage	V_{FB_O}			5.8		
FB pin short circuit current	V_{FB_S}	Short FB pin to gnd and measure current		0.9		mA
Burst mode FB threshold	$V_{FB\_th\_BM}$			1.7		V
Power limiting FB threshold	$V_{FB\_th\_P}$	Iout=－10mA		4.5		V
Power limiting delay time	T_PL_D			64		mA
OSCILLATOR						
Normal oscillation frequency	F_{OSC}		60	65	70	KHz
Frequency temperature stability	$\Delta f_{\_Temp}$	TA -20°C to +100°C		2		%
Frequency supply stability	$\Delta f_{\_Sup}$	VDD 12-25V		2		%
Operating RI range	$RI_{\_range}$		12	24	60	KΩ
RI open load voltage	R_{I_open}			2		V
Burst mode base frequency	$F_{OSC\text{-}BM}$			25		KHz
Frequency modulate range (jitter)	$\Delta f_{\_OSC}$		-5		5	%

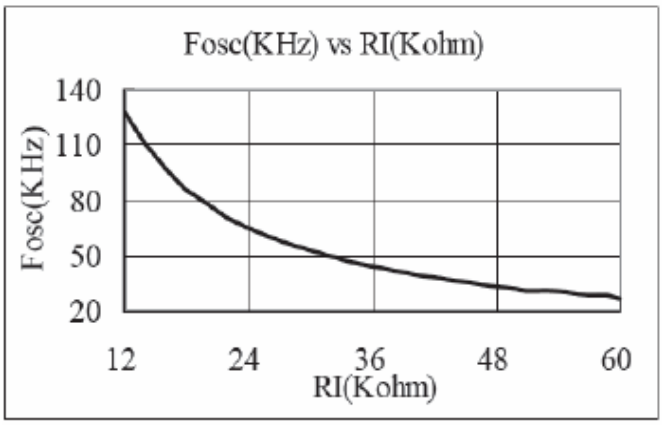
Maxim duty cycle	D_{MAX}	VDD=18V,FB=3V,SENSE=0V		80		%
Minimal duty cycle	D_{MIN}			0		%
Leading edge blanking time	T_{blank}			250	300	nS
Sense pin input impedance	R_{sense}			30		kΩ
Over current threshold voltage while no compensation	$V_{TH\_OC\_0}$	I(VIN)=0uA	0.85	0.90	0.95	V
Over current threshold voltage while compensation	$V_{TH\_OC\_1}$	I(VIN)=150uA		0.81		V
GATE OUTPUT						
Output low level	V_{OL}	VDD=18V,Io=-20mA			0.3	V
Output high level	V_{OH}	VDD=18V,Io=-20mA	11V			V
Output voltage clamped level	V_{G_CLP}			18		V
Output rising time	T_r	VDD=18V,Cl=1nf		110		nS
Output falling time	T_f	VDD=18V,Cl=1nf		40		nS
OVER TEMPERATURE PROTECTION						
Output current of RT pin	I_{RT}			70		uA
OTP threshold voltage	V_{TH_OTP}			0.65		V
OTP recovery voltage	$V_{TH\_OTP\_off}$			0.8		V
OTP debounce time	T_{D_OTP}			100		uS

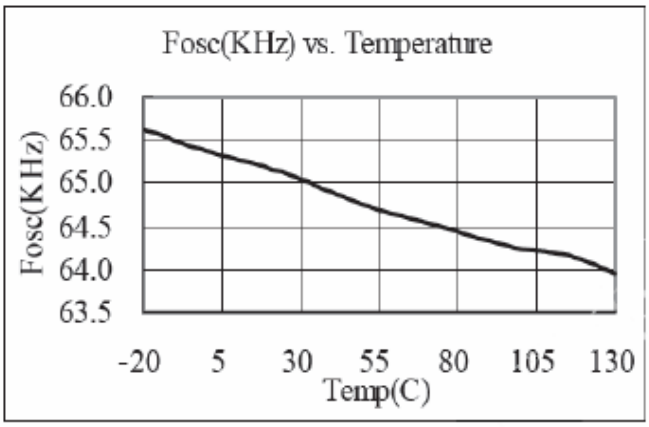
Characterization Plots

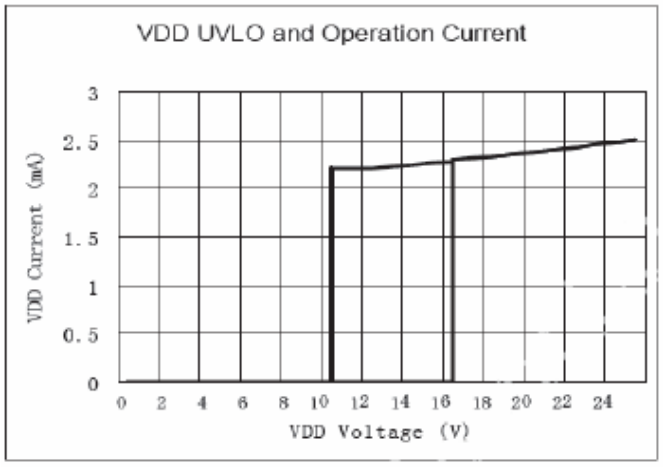
VDD = 16V, RI = 24 Kohm, TA = 25oC condition applies if not otherwise noted

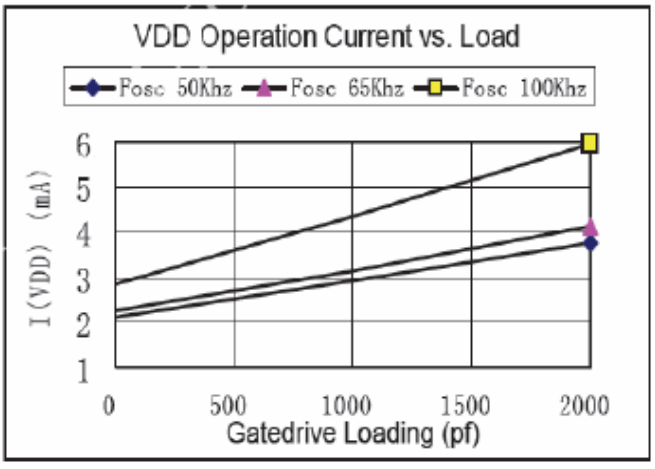


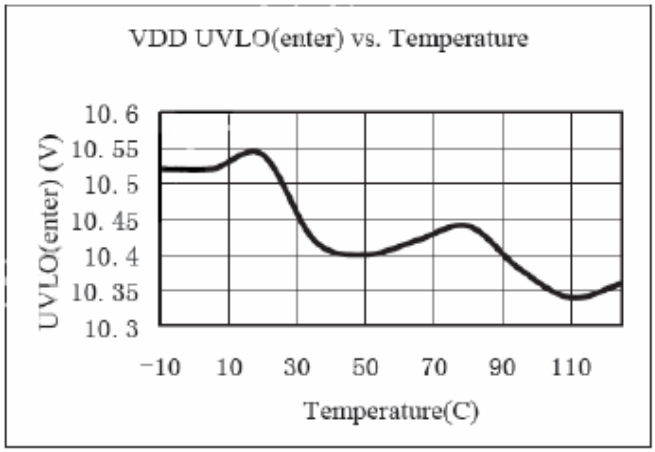


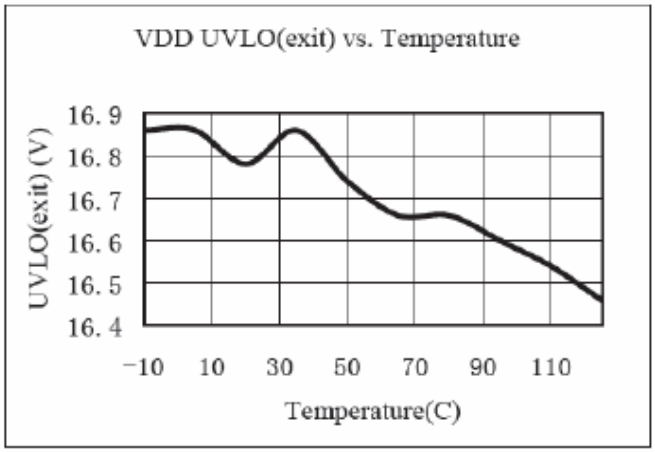


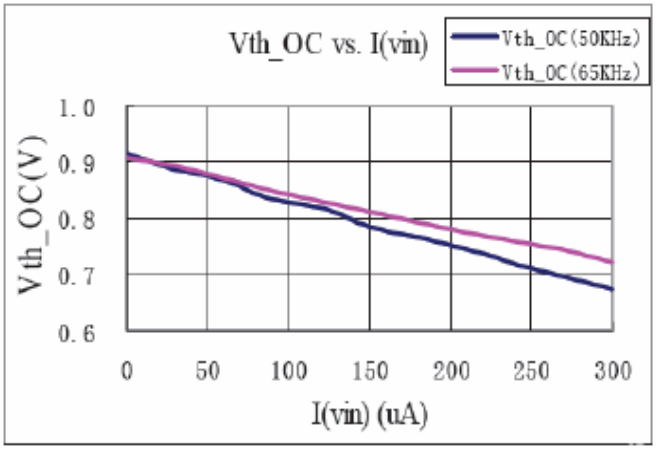


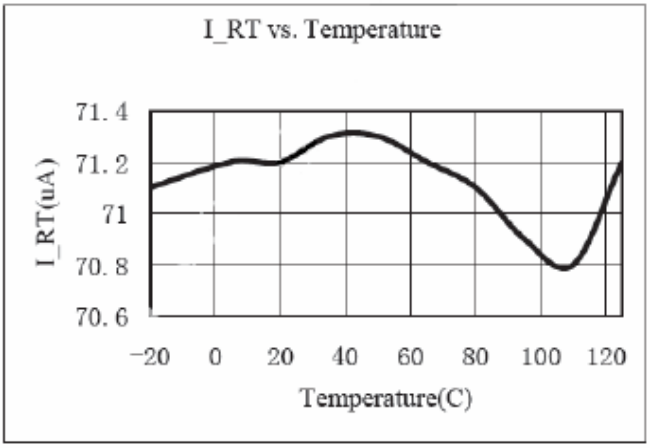




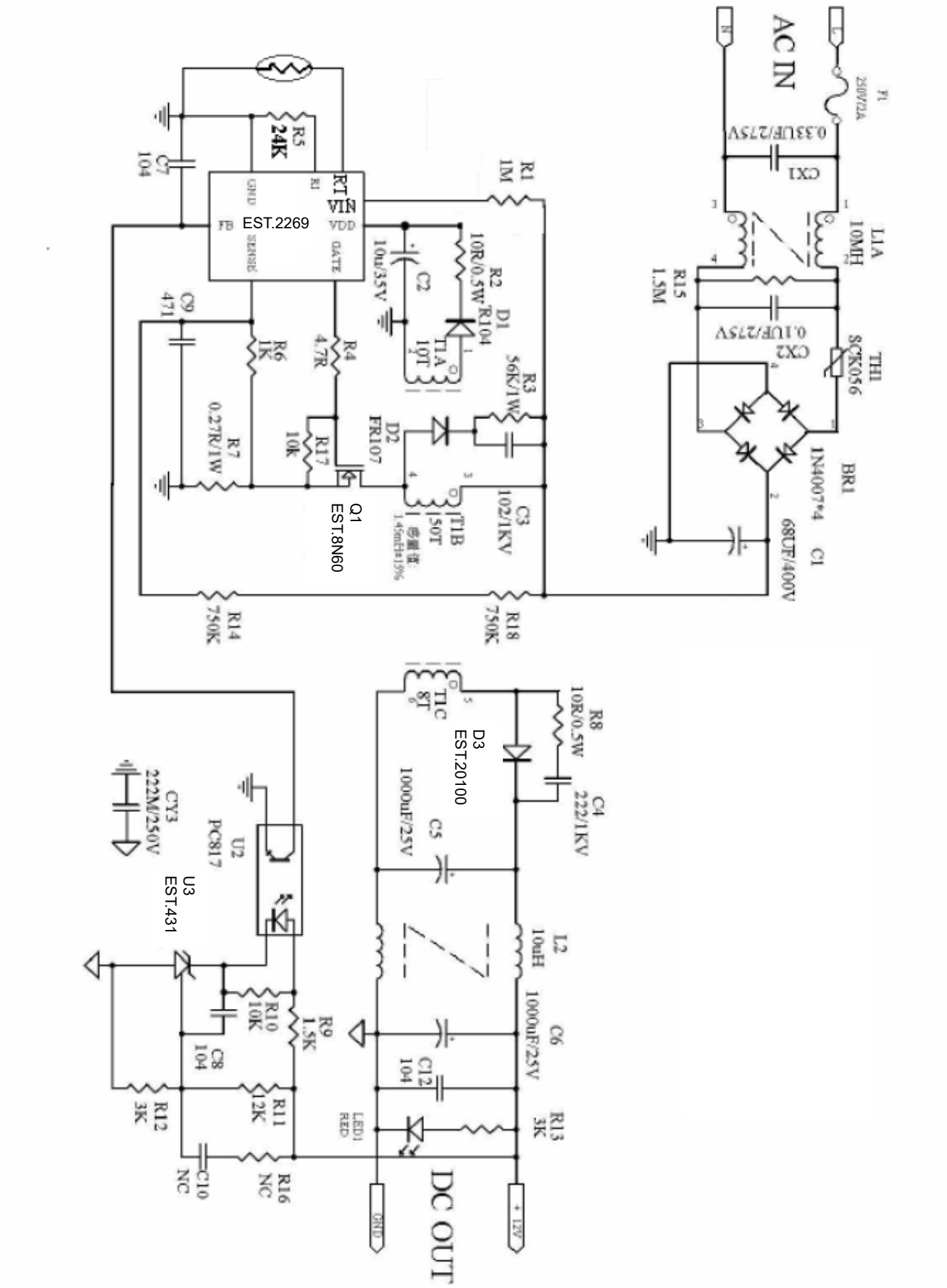

VDD UVLO(enter) vs. Temperature
UVLO(enter) (V)
10.6
10.55
10.5
10.45
10.4
10.35
10.3
−10
10
30
50
70
90
110
Temperature(C)


VDD UVLO(exit) vs. Temperature
UVLO(exit) (V)
16.9
16.8
16.7
16.6
16.5
16.4
−10
10
30
50
70
90
110
Temperature(C)


Vth_OC vs. I(vin)
Vth_OC(50KHz)
Vth_OC(65KHz)
Vth_OC(V)
1.0
0.9
0.8
0.7
0.6
0
50
100
150
200
250
300
I(vin) (uA)


I_RT vs. Temperature
I_RT(uA)
71.4
71.2
71
70.8
70.6
−20
0
20
40
60
80
100
120
Temperature(C)

Typical Performance Characteristics



Application Information

The EST.2269 is a highly integrated PWM controller IC optimized for offline flyback converter applications. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of EST.2269 is designed to be very low so that VDD could be charged up aboveUVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of EST.2269 is low at 2.3mA. Good efficiency is achieved with EST.2269 low operating current together with extended burst mode control schemes.

Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in EST.2269. The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out.The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET ransistor, the core loss of the transformer and theloss on the snubber circuit. The magnitude of power loss is in proportion to the number of swit--ching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

EST.2269 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off stateto minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$Fosc = 1560/RI(K\Omega)\ (Khz)$$

Current Sensing and Leading EdgeBlanking

Cycle-by-Cycle current limiting is offered in EST.2269 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than VTH_OTP.

Gate Drive

EST.2269 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

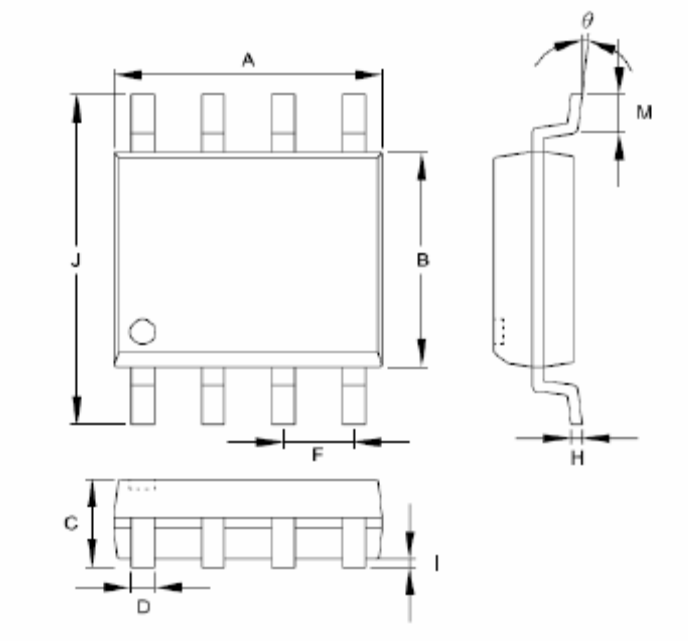
Protection Controls

Good system reliability is achieved with EST.2269's rich protection features including Cycle-by- Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on chip VDD over voltage protection (OVP, optional) and under voltage lockout (UVLO).

The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on EST2269.At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is Detected. EST.2269 resumes the operation when temperature drops below the hysteresis value. VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter

Package Information



SOP-8

Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°